

Micropower 300-mA CMOS LDO Regulator With Error Flag

FEATURES

- Input Voltage: 2.35–6.0 V
- Fixed 1.5-V, 1.8-V, 2.0-V, 2.5-V, 2.775-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V, or Adjustable Output Voltage Options
- Low 120-mV Dropout at 300-mA Load
- Guaranteed 300-mA Output Current
- 500-mA Peak Output Current Capability
- Uses Low ESR Ceramic Output Capacitor
- Fast Load and Line Transient Response
- Only 100- μ V(rms) Noise With Noise Bypass Capacitor

- 1- μ A Maximum Shutdown Current
- Built-in Short Circuit and Thermal Protection
- Out-Of-Regulation Error Flag (Power_Good)

APPLICATIONS

- Cellular Phones
- Laptop and Palm Computers
- PDA, Digital Still Cameras

DESCRIPTION

The Si91821 is a 300-mA CMOS LDO (low dropout) voltage regulator. The device features ultra low ground current and dropout voltage to prolong battery life in portable electronics. The Si91821 offers line and load transient response and ripple rejection superior to that of bipolar or BiCMOS LDO regulators. The device is designed to maintain regulation while delivering 500-mA peak current. This is useful for systems that have high surge current upon turn-on. The Si91821 is designed to drive the lower cost ceramic, as well as tantalum, output capacitors.

The device is guaranteed stable from maximum load current down to 0-mA load. In addition, an external noise bypass capacitor connected to the device's C_{NOISE} pin will lower the LDO's output noise for low noise applications.

The Si91821 also includes an out-of-regulation error flag. When the output voltage is 5% below its nominal output voltage, the error flag output goes low.

TYPICAL APPLICATIONS CIRCUITS

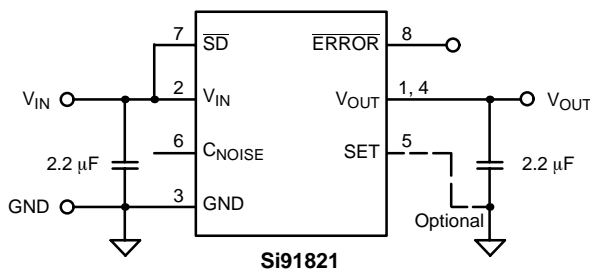


Figure 1. Fixed Output

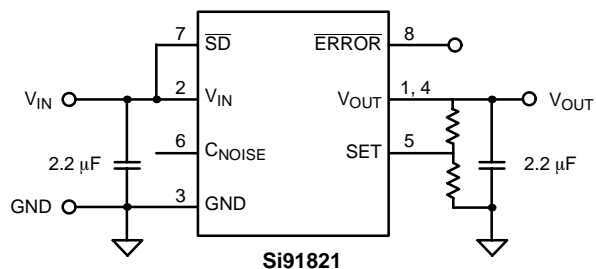


Figure 2.. Adjustable Output

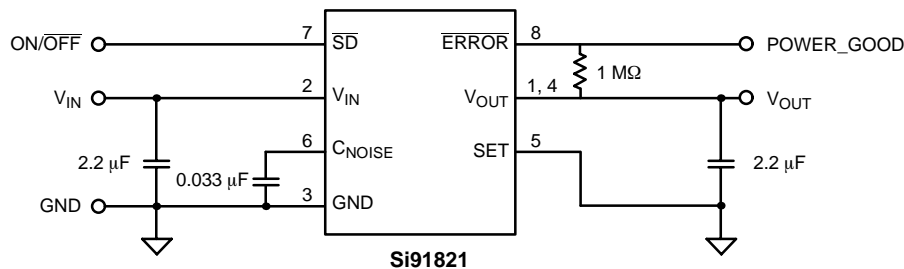


Figure 3. Fixed Output, Low Noise, Full Features Application

ABSOLUTE MAXIMUM RATINGS

Input Voltage, V_{IN}	6.5 V
SD Input Voltage, V_{SD}	-0.3 V to V_{IN}
Output Current, I_{OUT}	Short Circuit Protected
Output Voltage, V_{OUT}	-0.3 V to $V_{O(nom)} + 0.3$ V
Maximum Junction Temperature, $T_{J(max)}$	150°C
Storage Temperature, T_{STG}	-55°C to 150°C
ESD (Human Body Model)	2 kV

Power Dissipation (Package) ^a	
8-Pin MSOP ^b	666 mW
Thermal Impedance (Θ_{JA}) ^a	
8-Pin MSOP ^b	185°C/W

Notes

- a. Device mounted with all leads soldered or welded to PC board.
b. Derate 10 mW/°C above $T_A = 25^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Input Voltage, V_{IN}	2.35 V to 6 V	I_{OUT}	0 to 300 mA
Output Voltage, V_{OUT}	1.5 to 5.0 V	Operating Ambient Temperature, T_A	-40°C to 85°C
SD Input Voltage, V_{SD}	0 V to V_{IN}	Operating Junction Temperature, T_J	-40°C to 125°C

$C_{IN} = 2.2 \mu\text{F}$, $C_{OUT} = 2.2 \mu\text{F}$ (ceramic, X5R or X7R type), $C_{NOISE} = 0.033 \mu\text{F}$ (ceramic)

C_{OUT} Range = 1 μF to 10 μF ($\pm 10\%$, x5R or x7R type)

$C_{IN} \geq C_{OUT}$

SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA $C_{IN} = 2.2 \mu\text{F}$, $C_{OUT} = 2.2 \mu\text{F}$, $V_{SD} = 1.5$ V	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Input Voltage	V_{IN}			2.35		6.0	V
Output Voltage	V_{OUT}	Adjustable Version	Full	1.5		5.0	
Output Voltage Accuracy (to stated output voltage)	V_{OUT}	$1 \text{ mA} \leq I_{OUT} \leq 300 \text{ mA}$	Room	-1.5		1.5	%
			Full	-2.5		2.5	
Feedback Voltage (ADJ Version)	V_{SET}		Room	1.191	1.215	1.239	V
			Full	1.179		1.251	
Line Regulation (Except 5-V Version)	$\frac{\Delta V_{OUT} \times 100}{V_{IN} \times V_{OUT(nom)}}$	From $V_{IN} = V_{OUT(nom)} + 1$ V to $V_{OUT(nom)} + 2$ V	Full	-0.18		0.18	%V
Line Regulation (5-V Version)		From $V_{IN} = 5.5$ V to 6 V	Full	-0.18		0.18	
Line Regulation (ADJ Version)		$V_{OUT} = 1.5$ V From $V_{IN} = 2.5$ V to 3.5 V	Full	-0.18		0.18	
		$V_{OUT} = 5$ V From $V_{IN} = 5.5$ V to 6 V	Full	-0.18		0.18	
Dropout Voltage ^d	$V_{IN} - V_{OUT}$	$I_{OUT} = 10$ mA	Room		5	20	mV
		$I_{OUT} = 200$ mA	Full		80	135	
		$I_{OUT} = 300$ mA	Full		120	200	
Ground Pin Current	I_{GND}	$I_{OUT} = 0$ mA	Full		150	270	μA
		$I_{OUT} = 200$ mA	Room		500		
		$I_{OUT} = 300$ mA	Room		600		
Shutdown Supply Current	$I_{IN(off)}$	$V_{SD} = 0$ V	Room		0.1	1	
Peak Output Current	$I_{O(peak)}$	$V_{OUT} \geq 0.95 \times V_{OUT(nom)}$, $t_{pw} = 2$ ms	Room	500			mA
Output Noise Voltage	e_N	BW = 10 Hz to 100 kHz $I_{OUT} = 150$ mA	w/o C_{NOISE}	Room		260	$\mu\text{V (rms)}$
			$C_{NOISE} = 0.1 \mu\text{F}$	Room		37	
		BW = 10 to 100 kHz $I_{OUT} = 10$ mA	$C_{NOISE} = 33$ nF	Room		54	
Ripple Rejection	$\Delta V_{OUT}/\Delta V_{IN}$	$I_{OUT} = 150$ mA	f = 1 kHz	Room		60	dB
			f = 10 kHz	Room		50	
			f = 100 kHz	Room		40	



SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$ $C_{IN} = 2.2\text{ }\mu\text{F}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $V_{SD} = 1.5\text{ V}$	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Dynamic Line Regulation	$\Delta V_{O(line)}$	$V_{IN} : V_{OUT(nom)} + 1\text{ V}$ to $V_{OUT(nom)} + 2\text{ V}$ $t_r/t_f = 5\text{ }\mu\text{s}$, $I_{OUT} = 250\text{ mA}$	Room		10		mV
Dynamic Load Regulation	$\Delta V_{O(load)}$	$I_{OUT} : 1\text{ mA}$ to 150 mA , $t_r/t_f = 2\text{ }\mu\text{s}$	Room		30		
Turn-on Overshoot	ΔV_{OOS}	V_{IN} followed by $\overline{SD} = \text{High Event}$ $C_{NOISE} \leq 100\text{ nF}$	Room			2.5	%
V_{OUT} Turn-On-Time	t_{ON}	$C_{OUT} = 10\text{ }\mu\text{F}$, V_{OUT} to 90% of final value, $V_{IN} = 3.6\text{ V}$	Room		350		μs
Thermal Shutdown							
Thermal Shutdown Junction Temp	$T_{J(s/d)}$		Room		165		°C
Thermal Hysteresis	T_{HYST}		Room		20		
Short Circuit Current	I_{SC}	$V_{OUT} = 0\text{ V}$	Room		800		mA
Shutdown Input							
\overline{SD} Input Voltage	V_{IH}	High = Regulator ON (Rising)	Full	1.5		V_{IN}	V
	V_{IL}	Low = Regulator OFF (Falling)	Full			0.4	
\overline{SD} Input Current ^e	I_{IH}	$V_{SD} = 0\text{ V}$, Regulator OFF	Room		0.01		μA
	I_{IL}	$V_{SD} = 6\text{ V}$, Regulator ON	Room		1.0		
Shutdown Hysteresis	V_{HYST}		Full		100		mV
Error Output							
Output High Leakage	I_{OFF}	$\overline{ERROR} = V_{OUT(nom)}$	Full		0.01	2	μA
Output Low Voltage	V_{OL}	$I_{SINK} = 2\text{ mA}$	Full			0.4	
Power_Good Trip Threshold ^{f, g} (Rising)	V_{TH}		Full	$0.93 \times V_{OUT}$	$0.95 \times V_{OUT}$	$0.97 \times V_{OUT}$	V
Hysteresis ^f	V_{HYST}		Room		$2\% \times V_{OUT}$		
Error Delay	t_{DELAY}	$C_{NOISE} \leq 100\text{ nF}$	Full			10	μs

Notes

- a. Room = 25°C, Full = -40 to 85°C.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing and are measured at $T_A = 25^\circ\text{C}$.
- d. The dropout voltage is defined as $V_{IN} - V_{OUT}$ when V_{OUT} is 100 mV below the value of V_{OUT} for $V_{IN} = V_{OUT} + 2\text{ V}$. This is applicable for voltages of 2.5 V or higher.
- e. The device's shutdown pin includes a typical 6-M Ω internal pull-down resistor connected to ground.
- f. V_{OUT} is defined as the output voltage of the DUT at 1 mA.
- g. Typical only, from $V_{OUT} = 2.0\text{ V}$ to $V_{OUT} = 1.5\text{ V}$.

TIMING WAVEFORMS

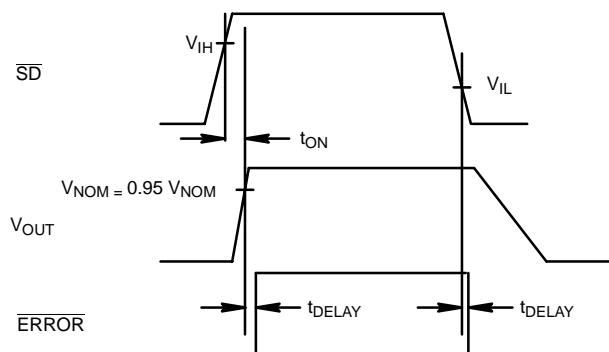
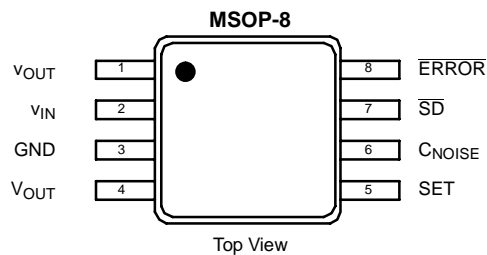


Figure 4. Timing Diagram for Power-Up

PIN CONFIGURATION



PIN DESCRIPTION

Pin Number	Name	Function
1, 4	V_{OUT}	Output voltage. Connect C_{OUT} between this pin and ground.
2	V_{IN}	Input supply pin. Bypass this pin with a 2.2- μ F ceramic or tantalum capacitor to ground.
3	GND	Ground pin. Local ground for C_{NOISE} and C_{OUT} .
5	SET	For fixed output voltage versions, this pin could be connected to GND. For adjustable output voltage version, this voltage feedback pin sets the output voltage via an external resistor divider.
6	C_{NOISE}	Noise bypass pin. For low noise applications, a 0.01- μ F or larger ceramic capacitor should be connected from this pin to ground.
7	\overline{SD}	By applying less than 0.4 V to this pin, the device will be turned off. Connect this pin to V_{IN} if unused.
8	\overline{ERROR}	This open drain output is an error flag output which goes low when V_{OUT} drops 5% below its nominal voltage.

BLOCK DIAGRAM

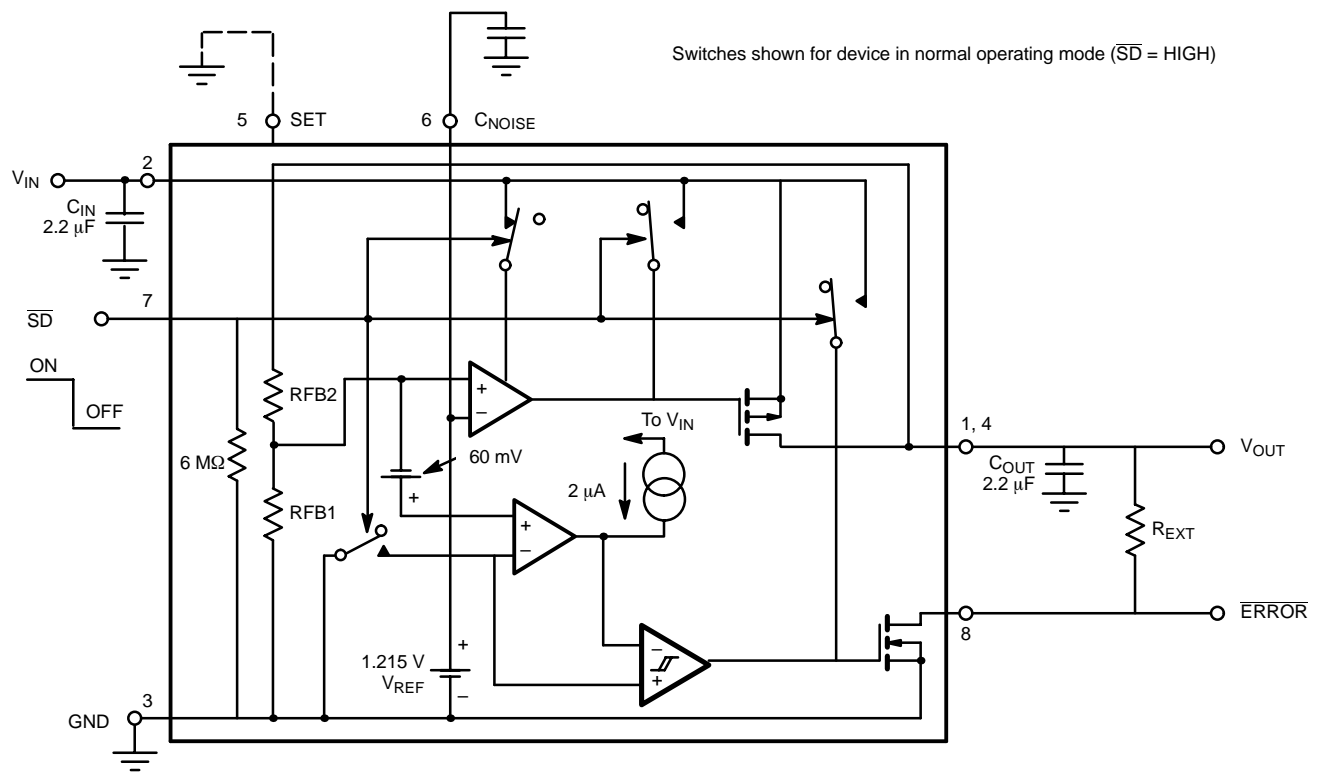


Figure 5. 300-mA CMOS LDO Regulator

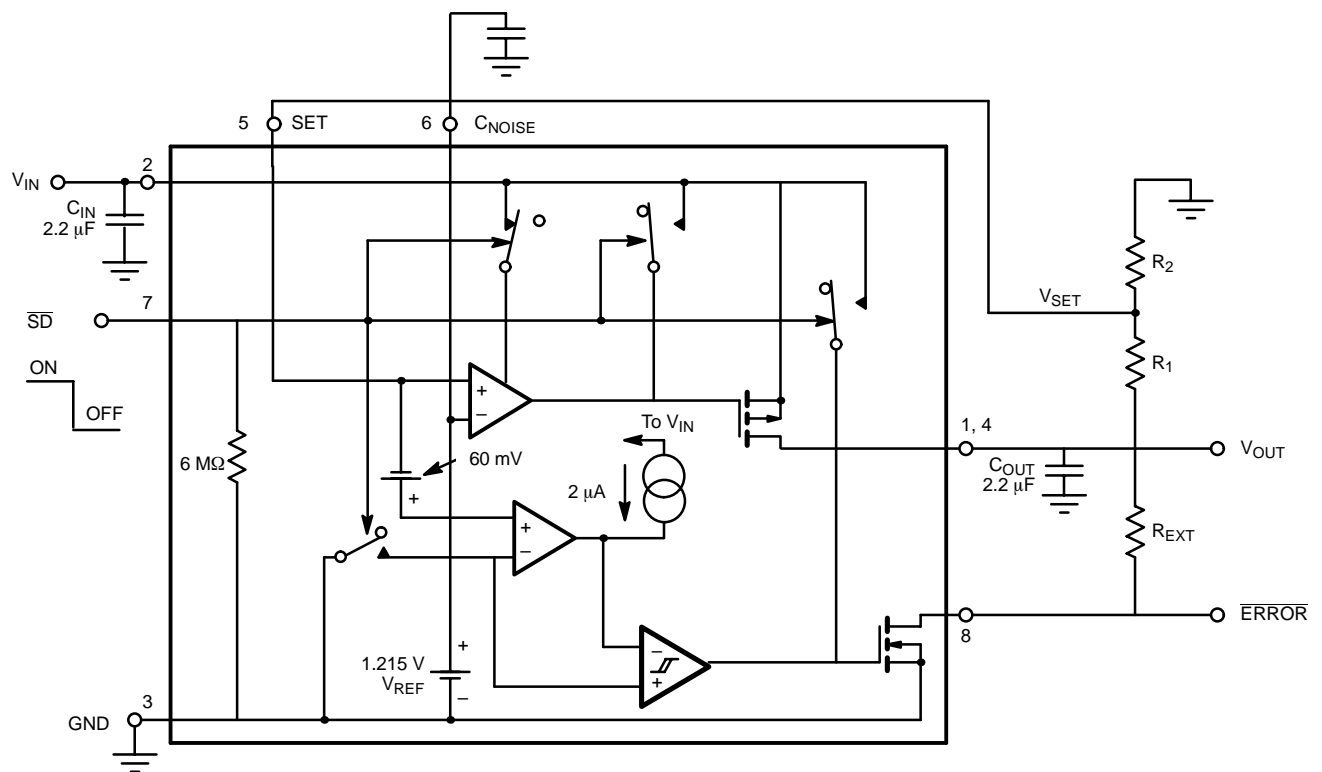


Figure 6. 300-mA CMOS LDO Regulator (Adjustable Output)



DETAILED DESCRIPTION

The Si91821 is a low drop out, low quiescent current, and very linear regulator with very fast transient response. It is primarily designed for battery powered applications where battery run time is at a premium. The low quiescent current allows extended standby time while low drop out voltage enables the system to fully utilize battery power before recharge. The Si91821 is a very fast regulator with bandwidth exceeding 50 kHz while maintaining low quiescent current at light load conditions. With this bandwidth, the Si91821 is the fastest LDO available today. The Si91821 is stable with any output capacitor type from 1 μ F to 10.0 μ F. However, X5R or X7R ceramic capacitors are recommended for best output noise and transient performance.

V_{IN}

V_{IN} is the input supply pin. The bypass capacitor for this pin is not critical as long as the input supply has low enough source impedance. For practical circuits, a 1.0- μ F or larger ceramic capacitor is recommended. When the source impedance is not low enough and/or the source is several inches from the Si91821, then a larger input bypass capacitor is needed. It is required that the equivalent impedance (source impedance, wire, and trace impedance in parallel with input bypass capacitor impedance) must be smaller than the input impedance of the Si91821 for stable operation. When the source impedance, wire, and trace impedance are unknown, it is recommended that an input bypass capacitor be used of a value that is equal to or greater than the output capacitor.

V_{OUT}

V_{OUT} is the output voltage of the regulator. Connect a bypass capacitor from V_{OUT} to ground. The output capacitor can be any value from 1.0 μ F to 10.0 μ F. A ceramic capacitor with X5R or X7R dielectric type is recommended for best output noise, line transient, and load transient performance.

GND

Ground is the common ground connection for V_{IN} and V_{OUT} . It is also the local ground connection for C_{NOISE} , SET, and \overline{SD} .

SET

SET is not connected internally for the fixed voltage version. Therefore, it can be connected to GND optionally. For the adjustable output version, use a resistor divider R_1 and R_2 , connect R_1 from V_{OUT} to SET and R_2 from SET to ground. R_2 should be in the 25-k Ω to 150-k Ω range for low power consumption, while maintaining adequate noise immunity.

The formula below calculates the value of R_1 , given the desired output voltage and the R_2 value.

$$R_1 = \frac{(V_{OUT} - V_{SET})R_2}{V_{SET}} \quad (1)$$

V_{SET} is nominally 1.215 V.

SHUTDOWN (\overline{SD})

\overline{SD} controls the turning on and off of the Si91821. V_{OUT} is guaranteed to be on when the \overline{SD} pin voltage equals or is greater than 1.5 V. V_{OUT} is guaranteed to be off when the \overline{SD} pin voltage equals or is less than 0.4 V. During shutdown mode, the Si91821 will draw less than 2- μ A current from the source. To automatically turn on V_{OUT} whenever the input is applied, tie the \overline{SD} pin to V_{IN} .

ERROR

\overline{ERROR} is an open drain output that goes low when V_{OUT} is less than 5% of its normal value. As with any open drain output, an external pull up resistor is needed. This function is active in shutdown.

The \overline{ERROR} pin must be left opened if not used.

C_{NOISE}

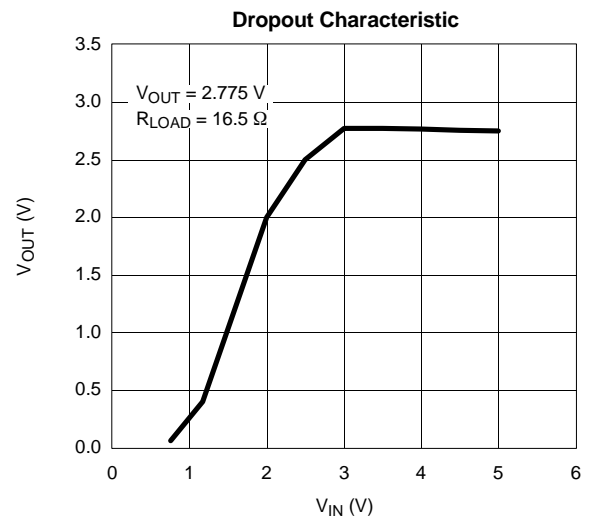
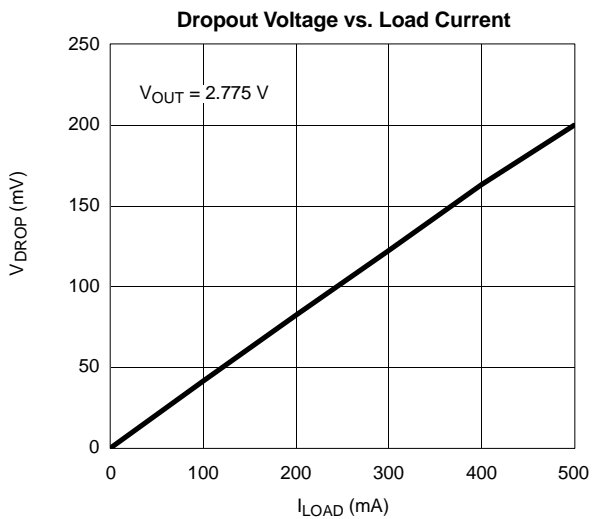
For low noise application, connect a high frequency ceramic capacitor from C_{NOISE} to ground. A 0.01- μ F or a 0.1- μ F X5R or X7R is recommended.



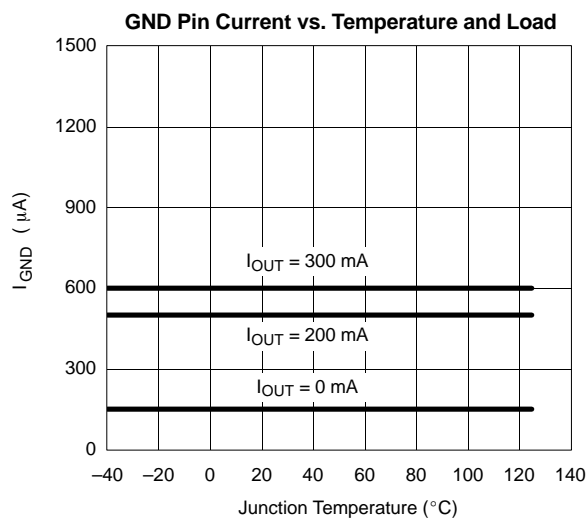
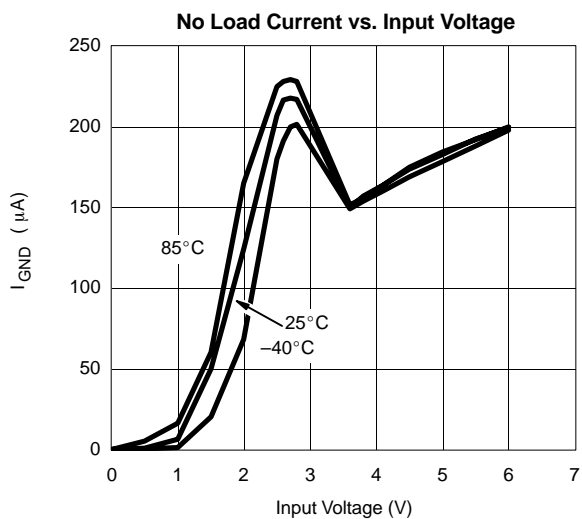
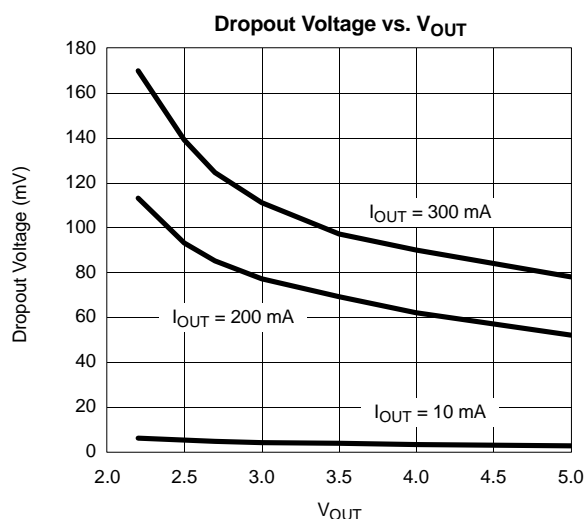
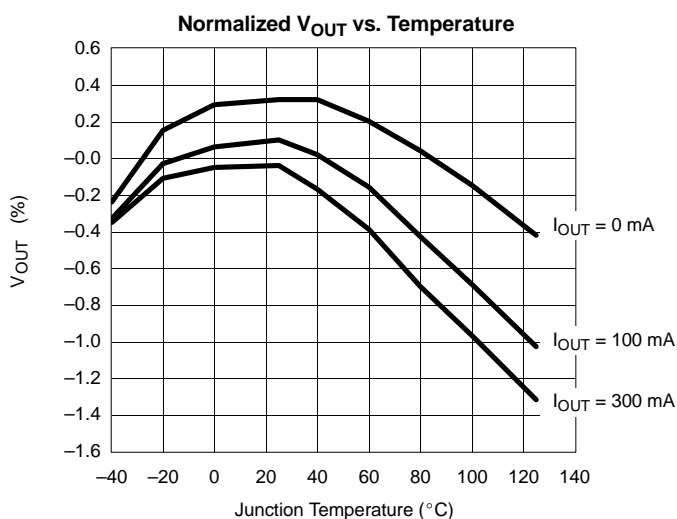
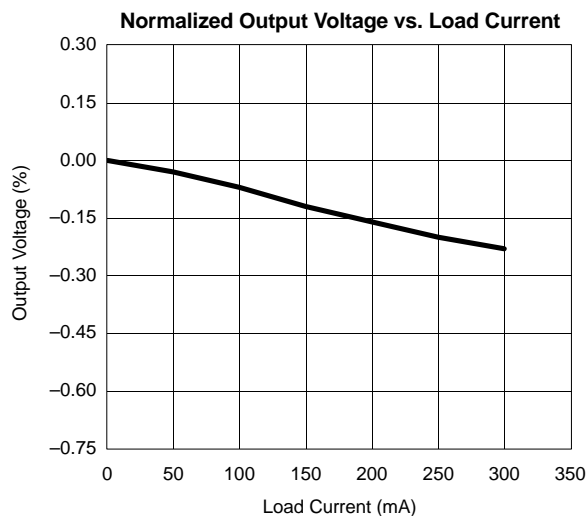
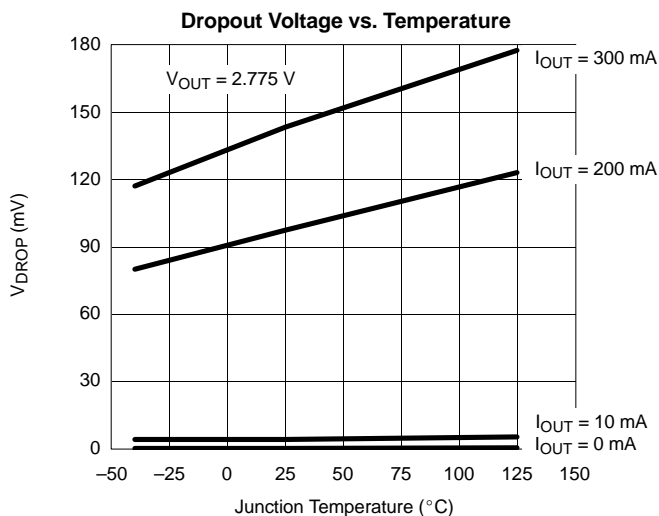
ORDERING INFORMATION				
Part Number	Marking	Voltage	Temperature Range	Package
Si91821DH-15-T1	1821 1500	1.50 V	-40 to 85°C	MSOP-8
Si91821DH-18-T1	1821 1800	1.80 V		
Si91821DH-20-T1	1821 2000	2.00 V		
Si91821DH-25-T1	1821 2500	2.50 V		
Si91821DH-277-T1	1821 2775	2.775 V		
Si91821DH-28-T1	1821 2800	2.80 V		
Si91821DH-30-T1	1821 3000	3.00 V		
Si91821DH-33-T1	1821 3300	3.30 V		
Si91821DH-50-T1	1821 5000	5.00 V		
Si91821DH-AD-T1	1821 ADJ	Adjustable		

Eval Kit	Temperature Range	Board Type
Si91821DB	-40 to 85°C	Surface Mount

TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)

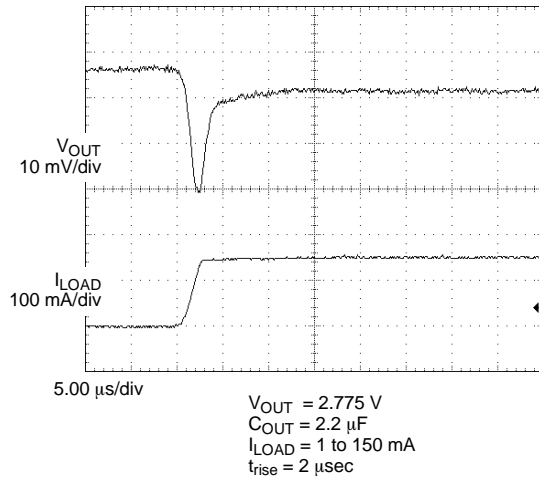


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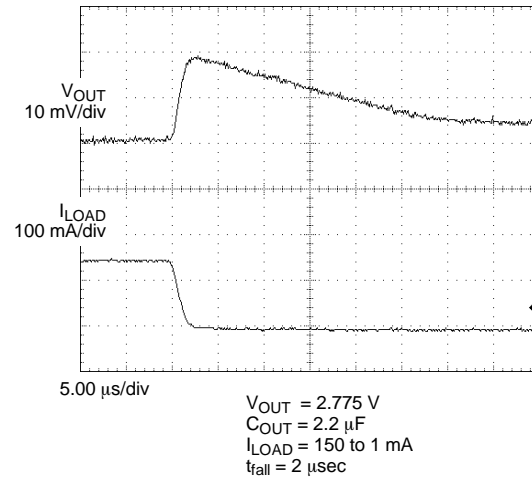


TYPICAL WAVEFORMS

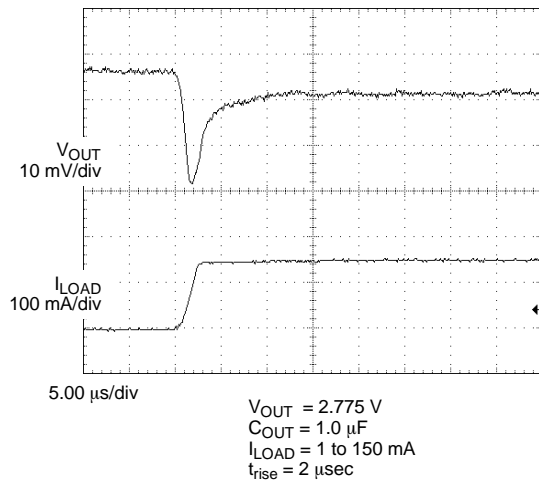
Load Transient Response-1



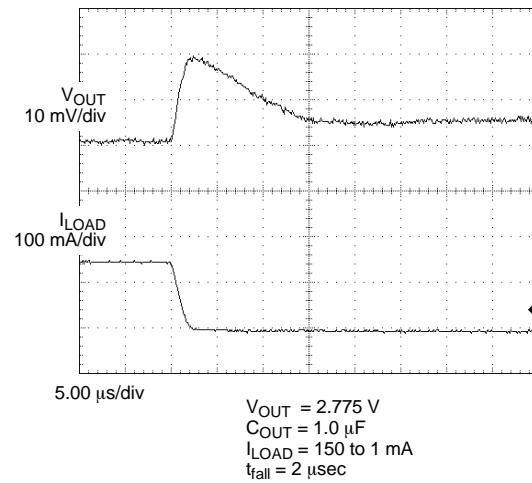
Load Transient Response-2



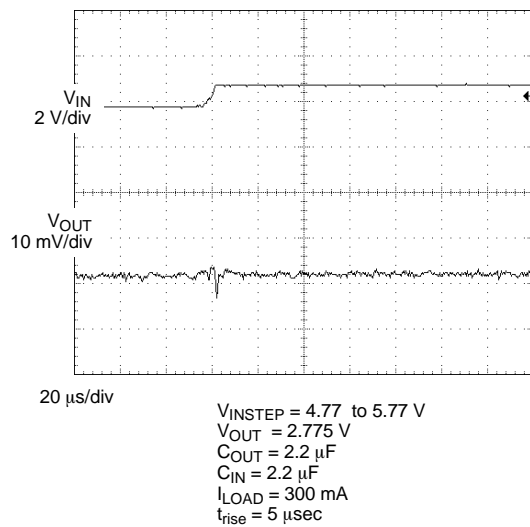
Load Transient Response-3



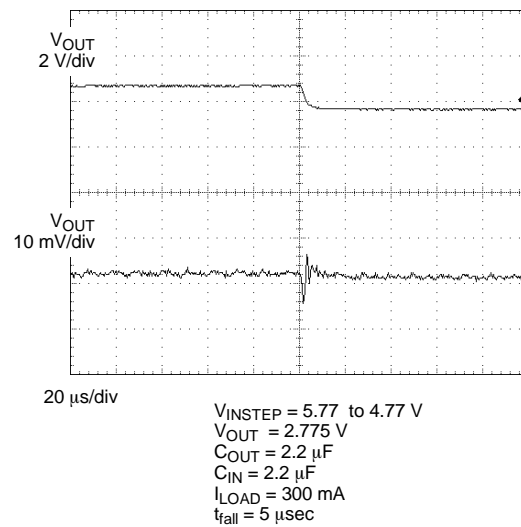
Load Transient Response-4



Line Transient Response-1



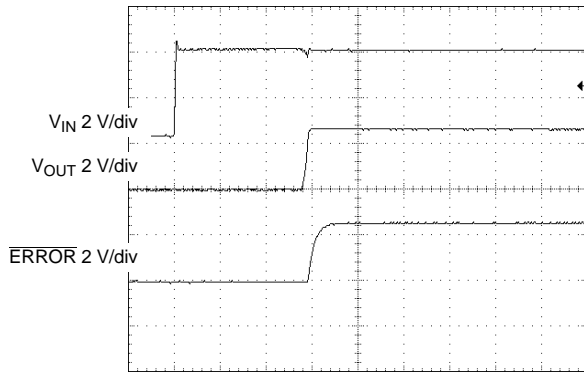
Line Transient Respons-2





TYPICAL WAVEFORMS

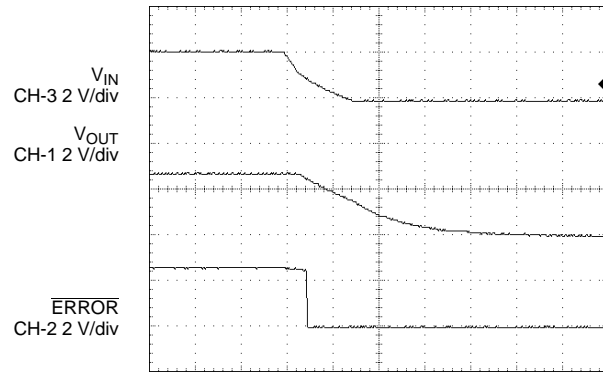
Turn-On Sequence



100 μ s/div

$V_{IN} = 4\text{ V}$
 $V_{OUT} = 2.775\text{ V}$
 $C_{NOISE} = 0.033\text{ }\mu\text{F}$
 $I_{LOAD} = 300\text{ mA}$

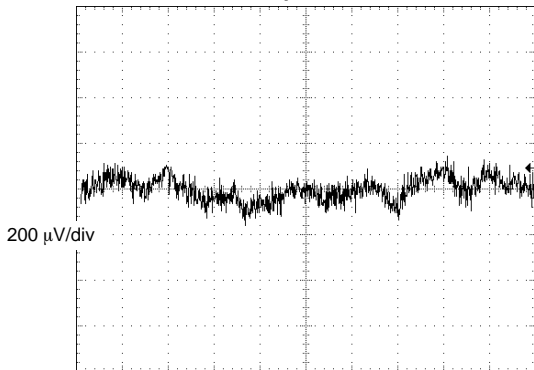
Turn-Off Sequence



20 μ s/div

$V_{IN} = 4\text{ V}$
 $V_{OUT} = 2.775\text{ V}$
 $C_{NOISE} = 0.033\text{ }\mu\text{F}$
 $I_{LOAD} = 300\text{ mA}$

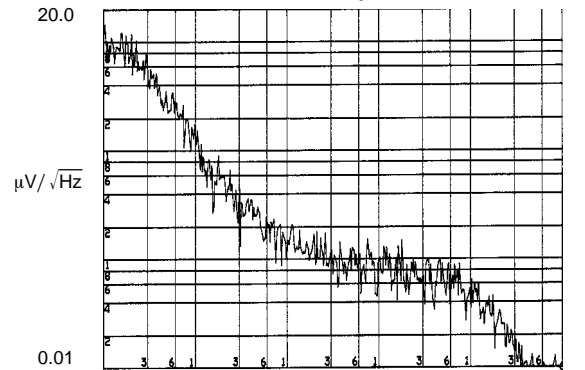
Output Noise



10 ms/div

$V_{IN} = 3.80\text{ V}$
 $V_{OUT} = 2.775\text{ V}$
 $I_{OUT} = 300\text{ mA}$
 $C_{NOISE} = 0.033\text{ }\mu\text{F}$
 $BW = 10\text{ Hz to }1\text{ MHz}$

Noise Spectrum



10 Hz

$V_{IN} = 3.80\text{ V}$
 $V_{OUT} = 2.775\text{ V}/10\text{ mA}$
 $C_{NOISE} = 0.033\text{ }\mu\text{F}$

1 MHz