Document Title

32M x 8 Bit NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial issue.	July 17th 2000	Advanced Information
0.1	1. Support copy-back program - The copy-back program is configured to quickly and efficiently rewrite data stored in one page within the array to another page within the same array without utilizing an external memory. Since the time-consuming sequently-reading and its re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated so that the rest of the block also need to be copied to the newly assigned free block.	Oct. 4th 2000	Preliminary
0.2	1. Explain how pointer operation works in detail. 2. For partial page programming into the copied page - Once the copy-back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. 3. Renamed GND input (pin # 6) on behalf of $\overline{SE}$ (pin # 6) - The $\overline{SE}$ input controls the access of the spare area. When $\overline{SE}$ is high, the spare area is not accessible for reading or programming. $\overline{SE}$ is recommended to be coupled to GND or Vcc and should not be toggled during reading or programming. => Connect this input pin to GND or set to static low state unless the sequential read mode excluding spare area is used. 4. Updated operation for tRST timing - If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.	Nov. 20th 2000	Preliminary
0.3	1. In addition, explain $\overline{WE}$ function in pin description - The $\overline{WE}$ must be held high when outputs are activated.	Mar. 2th 2001	
0.4	1.Powerup sequence is added : Recovery time of minimum 1μs is required before internal circuit gets ready for any command sequences	Jul. 22th 2001	

2. AC parameter tCLR(CLE to $\overline{RE}$ Delay, min 50ns) is added.
3. AC parameter tAR1 value : 100ns --> 20ns

Note : For more detailed features and specifications including FAQ, please refer to Samsung's Flash web site.
http://www.intl.samsungsemi.com/Memory/Flash/datasheets.html

32M x 8 Bit NAND Flash Memory

FEATURES

- Voltage Supply : 2.7V~3.6V
- Organization
  - Memory Cell Array : (32M + 1024K)bit x 8bit
  - Data Register : (512 + 16)bit x8bit
- Automatic Program and Erase
  - Page Program : (512 + 16)Byte
  - Block Erase : (16K + 512)Byte
- 528-Byte Page Read Operation
  - Random Access : 10μs(Max.)
  - Serial Page Access : 50ns(Min.)
- Fast Write Cycle Time
  - Program time : 200μs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Intelligent Copy-Back
- Package :
  - K9F5608U0A-YCB0/YIB0 :
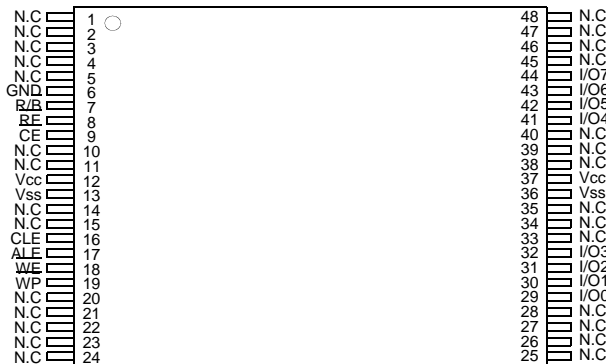   48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)

GENERAL DESCRIPTION

The K9F5608U0A are a 32M(33,554,432)x8bit NAND Flash Memory with a spare 1,024K(1,048,576)x8bit. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation programs the 528-byte page in typical 200μs and an erase operation can be performed in typical 2ms on a 16K-byte block. Data in the page can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command inputs. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9F5608U0A′s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm.

The K9F5608U0A-YCB0/YIB0 is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

PIN CONFIGURATION

K9F5608U0A-YCB0/YIB0

Left pin	#		#	Right pin
N.C	1		48	N.C
N.C	2		47	N.C
N.C	3		46	N.C
N.C	4		45	N.C
N.C	5		44	I/O7
GND	6		43	I/O6
R/B	7		42	I/O5
RE	8		41	I/O4
CE	9		40	N.C
N.C	10		39	N.C
N.C	11		38	N.C
Vcc	12		37	Vcc
Vss	13		36	Vss
N.C	14		35	N.C
N.C	15		34	N.C
CLE	16		33	N.C
ALE	17		32	I/O3
WE	18		31	I/O2
WP	19		30	I/O1
N.C	20		29	I/O0
N.C	21		28	N.C
N.C	22		27	N.C
N.C	23		26	N.C
N.C	24		25	N.C

PIN DESCRIPTION

Pin Name	Pin Function
I/O0 ~ I/O7	Data Input/Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
CE	Chip Enable
RE	Read Enable
WE	Write Enable
WP	Write Protect
GND	GND input for enabling spare area
R/B	Ready/Busy output
Vcc	Power
Vss	Ground
N.C	No Connection

NOTE : Connect all Vcc and Vss pins of each device to common power supply outputs.
Do not leave Vcc or Vss disconnected.
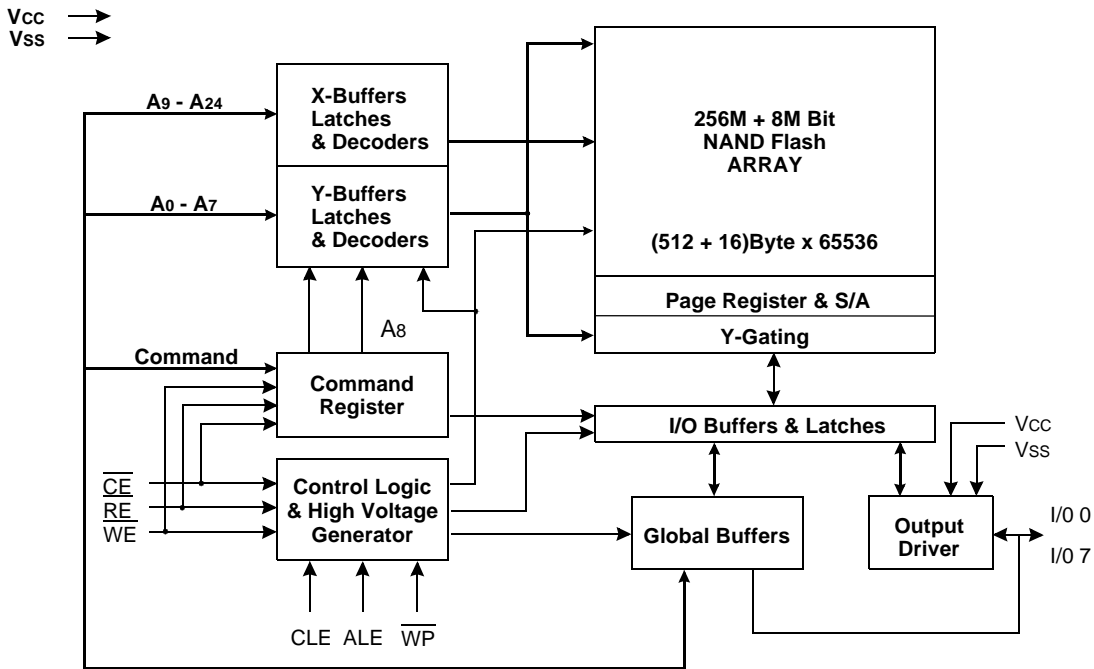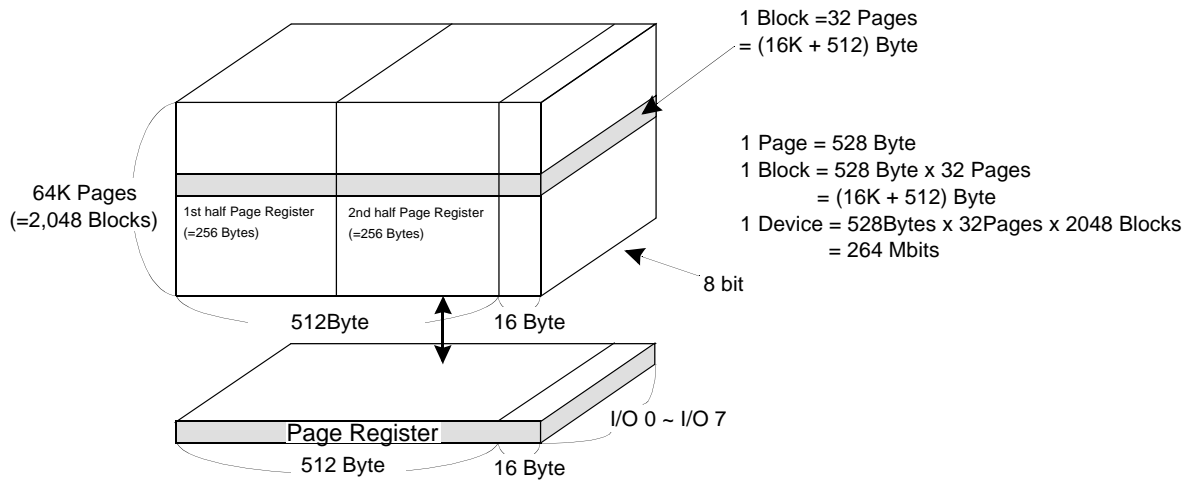
Figure 1. FUNCTIONAL BLOCK DIAGRAM

Figure 2. ARRAY ORGANIZATION

1 Block =32 Pages
= (16K + 512) Byte

1 Page = 528 Byte
1 Block = 528 Byte x 32 Pages
      = (16K + 512) Byte
1 Device = 528Bytes x 32Pages x 2048 Blocks
      = 264 Mbits

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	**Column Address**
2nd Cycle	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	**Row Address**
3rd Cycle	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	**(Page Address)**

NOTE : Column Address : Starting Address of the Register.

      00h Command(Read) : Defines the starting address of the 1st half of the register.

      01h Command(Read) : Defines the starting address of the 2nd half of the register.

      * A_8 is set to "Low" or "High" by the 00h or 01h Command.

      * The device ignores any additional input of address cycles than reuired.

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PRODUCT INTRODUCTION

The K9F5608U0A is a 264Mbit(276,824,064 bit) memory organized as 65,536 rows(pages) by 528 columns. Spare sixteen columns are located from column address of 512 to 527. A 528-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of the 32 pages formed by two NAND structures, totaling 8448 NAND structures of 16 cells. The array organization is shown in Figure 2. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 2048 separately erasable 16K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the K9F5608U0A.

The K9F5608U0A has addresses multiplexed into 8 I/O's. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except for Block Erase command which requires two cycles: one cycle for erase-setup and another for erase-execution after block address loading. The 32M byte physical space requires 25 addresses, thereby requiring three cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following the required command input. In Block Erase operation, however, only the two row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9F5608U0A.

Table 1. COMMAND SETS

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read 1	00h/01h[1]	-	
Read 2	50h[2]	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	00h	8Ah	
Block Erase	60h	D0h	
Read Status	70h	-	O

NOTE : 1. The 00h command defines starting address of the 1st half of registers.

The 01h command defines starting address of the 2nd half of registers.

After data access on the 2nd half of register by the 01h command, the status pointer is

automatically moved to the 1st half register(00h) on the next cycle.

2. The 50h command is valid only when the GND input(pin # 6) is low level.

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

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PIN DESCRIPTION

Command Latch Enable(CLE)

The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{\text{WE}}$ signal.

Address Latch Enable(ALE)

The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{\text{WE}}$ with ALE high.

Chip Enable($\overline{\text{CE}}$)

The $\overline{\text{CE}}$ input is the device selection control. When $\overline{\text{CE}}$ goes high during a read operation the device is returned to standby mode. However, when the device is in the Busy state during program or erase, $\overline{\text{CE}}$ high is ignored, and does not return the device to standby mode.

Write Enable($\overline{\text{WE}}$)

The $\overline{\text{WE}}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{\text{WE}}$ pulse.
The $\overline{\text{WE}}$ must be held high when outputs are activated.

Read Enable($\overline{\text{RE}}$)

The $\overline{\text{RE}}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{\text{RE}}$ which also increments the internal column address counter by one.

GND (Pin # 6)

Connect this input pin to GND or set to static low state unless the sequential read mode excluding spare area is used.

I/O Port : I/O 0 ~ I/O 7

The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.

Write Protect($\overline{\text{WP}}$)

The $\overline{\text{WP}}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{\text{WP}}$ pin is active low.

Ready/Busy($\overline{\text{R/B}}$)

The $\overline{\text{R/B}}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to Vss		V_{IN}	-0.6 to + 4.6	V
		V_{CC}	-0.6 to + 4.6	
Temperature Under Bias	K9F5608U0A-YCB0	T_{BIAS}	-10 to +125	°C
	K9F5608U0A-YIB0		-40 to +125	
Storage Temperature	K9F5608U0A-YCB0	T_{STG}	-65 to +150	°C
	K9F5608U0A-YIB0			

NOTE :
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions
   as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, K9F5608U0A-YCB0 :T_A=0 to 70°C, K9F5608U0A-YIB0:T_A=-40 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Sequential Read	I_{CC1}	t_{RC}=50ns, $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	10	20	mA
	Program	I_{CC2}	-	-	10	20	
	Erase	I_{CC3}	-	-	10	20	
Stand-by Current(TTL)		I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{WP}$=GND input (Pin #6) = 0V/V_{CC}	-	-	1	
Stand-by Current(CMOS)		I_{SB2}	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=GND input (Pin #6) = 0V/V_{CC}	-	10	50	μA
Input Leakage Current		I_{LI}	V_{IN}=0 to 3.6V	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to 3.6V	-	-	±10	
Input High Voltage		V_{IH}	-	2.0	-	V_{CC}+0.3	V
Input Low Voltage, All inputs		V_{IL}	-	-0.3	-	0.8	
Output High Voltage Level		V_{OH}	I_{OH}=-400μA	2.4	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=2.1mA	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	mA

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VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	2013	-	2048	Blocks

NOTE :
1. The K9F5608U0A may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for a appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

AC TEST CONDITION

(K9F5608U0A-YCB0 :TA=0 to 70°C, K9F5608U0A-YIB0:TA=-40 to 85°C, VCC=2.7V~3.6V unless otherwise)

Parameter	Value
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load (3.0V +/-10%)	1 TTL GATE and CL=50pF
Output Load (3.3V +/-10%)	1 TTL GATE and CL=100pF

CAPACITANCE(TA=25°C, VCC=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	GND	$\overline{WP}$	Mode	
H	L	L	⌐_⌐	H	X	X	Read Mode	Command Input
L	H	L	⌐_⌐	H	X	X		Address Input(3clock)
H	L	L	⌐_⌐	H	X	H	Write Mode	Command Input
L	H	L	⌐_⌐	H	X	H		Address Input(3clock)
L	L	L	⌐_⌐	H	L/H[3]	H	Data Input	
L	L	L	H	⌐_⌐	L/H[3]	X	Sequential Read & Data Output	
L	L	L	H	H	L/H[3]	X	During Read(Busy)	
X	X	X	X	X	L/H[3]	H	During Program(Busy)	
X	X	X	X	X	X	H	During Erase(Busy)	
X	X[1]	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc[2]	0V/Vcc[2]	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
         2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.
         3. When GND input is high, spare area is deselected.

Program/Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	500	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	2	cycles
	Spare Array		-	-	3	cycles
Block Erase Time		t_{BERS}	-	2	3	ms

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
$\overline{CE}$ Setup Time	t_{CS}	0	-	ns
$\overline{CE}$ Hold Time	t_{CH}	10	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	25[1]	-	ns
ALE Setup Time	t_{ALS}	0	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	50	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	-	ns

NOTE : 1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	10	μs
ALE to $\overline{RE}$ Delay(ID read)	t_{AR1}	20	-	ns
ALE to $\overline{RE}$ Delay(Read cycle)	t_{AR2}	50	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	50	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	30	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	50	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	35	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	15	30	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	20	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
Last RE High to Busy(at sequential read)	t_{RB}	-	100	ns
$\overline{CE}$ High to Ready(in case of interception by $\overline{CE}$ at read)	t_{CRY}	-	50 +tr(R/$\overline{B}$)[1]	ns
$\overline{CE}$ High Hold Time(at the last serial read)[2]	t_{CEH}	100	-	ns
$\overline{CE}$ Low to Status Output	t_{CEA}	-	45	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	ns
$\overline{RE}$ access time(Read ID)	t_{READID}	-	35	ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	5/10/500[3]	μs

NOTE :
1. The time to Ready depends on the value of the pull-up resistor tied R/$\overline{B}$ pin.
2. To break the sequential read cycle, $\overline{CE}$ must be held high for longer time than tCEH.
3. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.

NAND Flash Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. Devices with invalid block(s) have the same quality level or as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

Identifying Invalid Block(s)

All device locations are erased(FFh) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 6th byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every invalid block has non-FFh data at the column address of 517. Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 1). Any intentional erasure of the original invalid block information is prohibited.
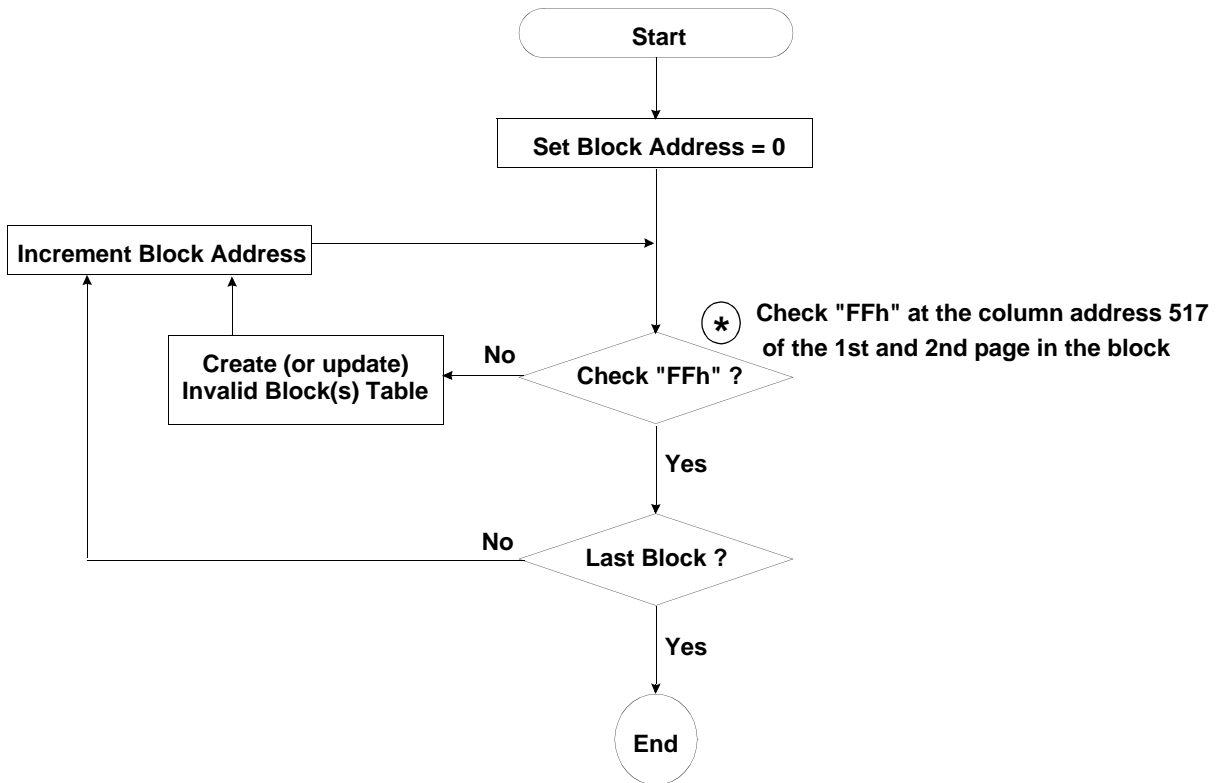
Figure 1. Flow chart to create invalid block table.

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NAND Flash Technical Notes *(Continued)*

Error in write or read operation

Over its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement or ECC Correction
Read	Single Bit Failure	Verify ECC -> ECC Correction

ECC   : Error Correcting Code --> Hamming Code etc.
                   Example) 1bit correction & 2bit detection

Program Flow Chart

If ECC is used, this verification operation is not needed.

Start → Write 80h → Write Address → Write Data → Write 10h → Read Status Register → I/O 6 = 1 ? or R/B = 1 ? (No loops back) → Yes → I/O 0 = 0 ? (No → Program Error *) → Yes

Write 00h → Write Address → Wait for tR Time → Verify Data (No → Program Error *) → Yes → Program Completed

* : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

Start

↓

Write 60h

↓

Write Block Address

↓

Write D0h

↓

Read Status Register

↓

I/O 6 = 1 ?
or R/B̄ = 1 ?   **No** →

↓ **Yes**

(*) **No** ← I/O 0 = 0 ?

Erase Error

↓ **Yes**

Erase Completed

Read Flow Chart

Start

↓

Write 00h

↓

Write Address

↓

Read Data

↓

ECC Generation

↓

No ← Verify ECC

Reclaim the Error

↓ **Yes**

Page Read Completed
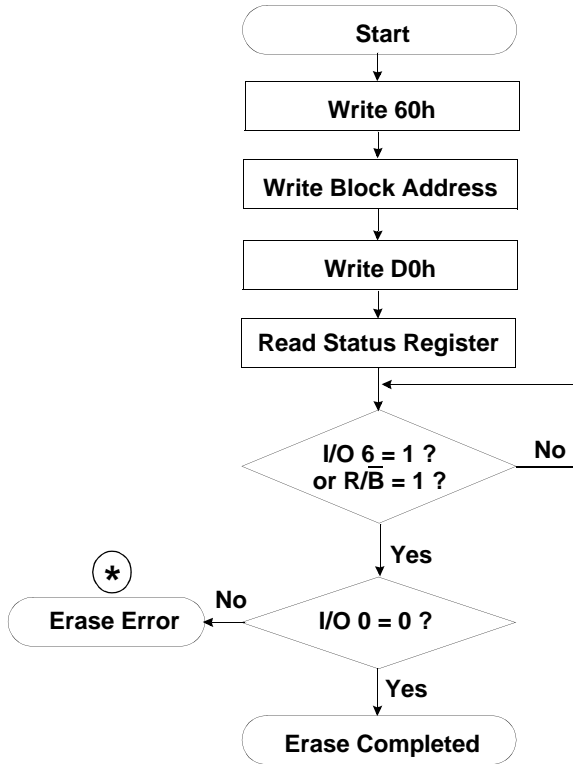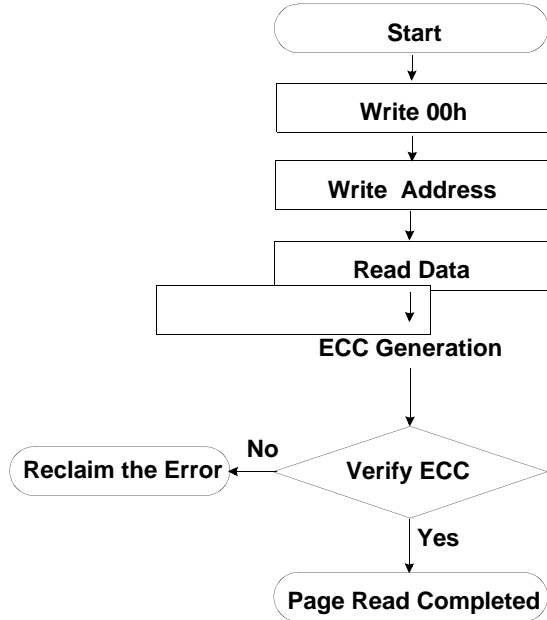
(*) : **If erase operation results in an error, map out
the failing block and replace it with another block.**

Block Replacement

Block A

1st
~
(n-1)th

nth → **an error occurs.**

(page)

②

Buffer memory of the controller.

Block B

1st
~
(n-1)th

nth →

(page)

①
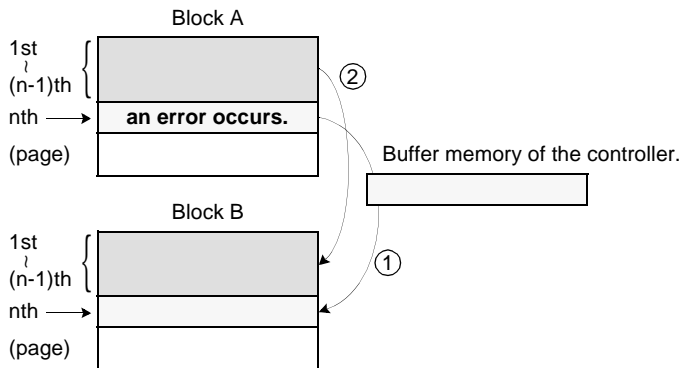
* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the nth page data of the Block 'A' in the buffer memory to the nth page of another free block. (Block 'B')
* Step3
Then, copy the data in the 1st ~ (n-1)th page to the same location of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

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Pointer Operation of K9F5608U0A

Samsung NAND Flash has three address pointer commands as a substitute for the two most significant column addresses. '00h' command sets the pointer to 'A' area(0~255byte), '01h' command sets the pointer to 'B' area(256~511byte), and '50h' command sets the pointer to 'C' area(512~527byte). With these commands, the starting column address can be set to any of a whole page(0~527byte). '00h' or '50h' is sustained until another address pointer command is inputted. '01h' command, however, is effective only for one operation. After any operation of Read, Program, Erase, Reset, Power_Up is executed once with '01h' command, the address pointer returns to 'A' area by itself. To program data starting from 'A' or 'C' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary. To program data starting from 'B' area, '01h' command must be inputted right before '80h' command is written.

Table 1. Destination of the pointer

Command	Pointer position	Area
00h	0 ~ 255 byte	1st half array(A)
01h	256 ~ 511 byte	2nd half array(B)
50h	512 ~ 527 byte	spare array(C)
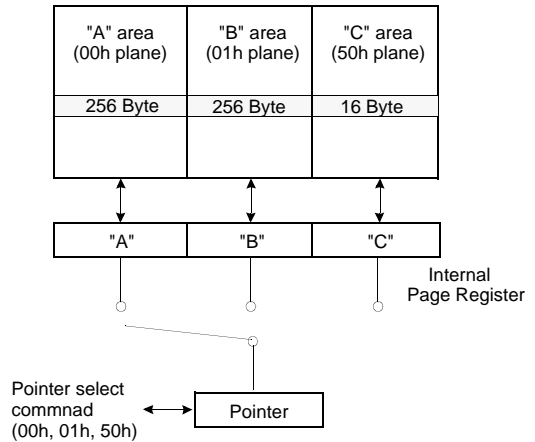
Figure 2. Block Diagram of Pointer Operation

(1) Command input sequence for programming 'A' area

The address pointer is set to 'A' area(0~255), and sustained

Address / Data input   Address / Data input

00h — 80h — 10h — (00h) — 80h — 10h

'A','B','C' area can be programmed.   '00h' command can be omitted.
It depends on how many data are inputted.
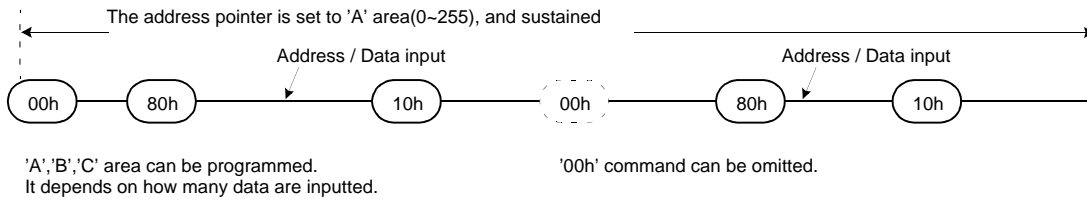
(2) Command input sequence for programming 'B' area

The address pointer is set to 'B' area(256~512), and will be reset to 'A' area after every program operation is executed.

Address / Data input   Address / Data input

01h — 80h — 10h — (01h) — 80h — 10h

'B', 'C' area can be programmed.   '01h' command must be rewritten before
It depends on how many data are inputted.   every program operation
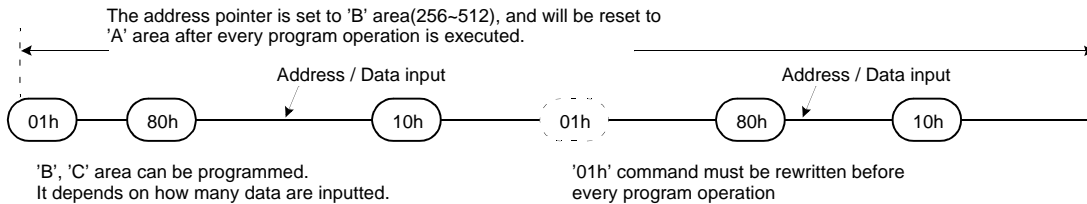
(3) Command input sequence for programming 'C' area

The address pointer is set to 'C' area(512~527), and sustained

Address / Data input   Address / Data input

50h — 80h — 10h — (50h) — 80h — 10h

Only 'C' area can be programmed.   '50h' command can be omitted.
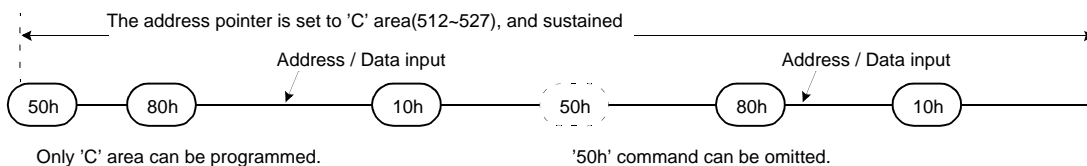
System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or sequential data-reading as shown below. The internal 528byte page registers are utilized as seperate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant savings in power consumption.

Figure 3. Program Operation with $\overline{CE}$ don't-care.

Timing requirements : If $\overline{CE}$ is is exerted high during data-loading, tCS must be minimum 10ns and tWC must be increased accordingly.
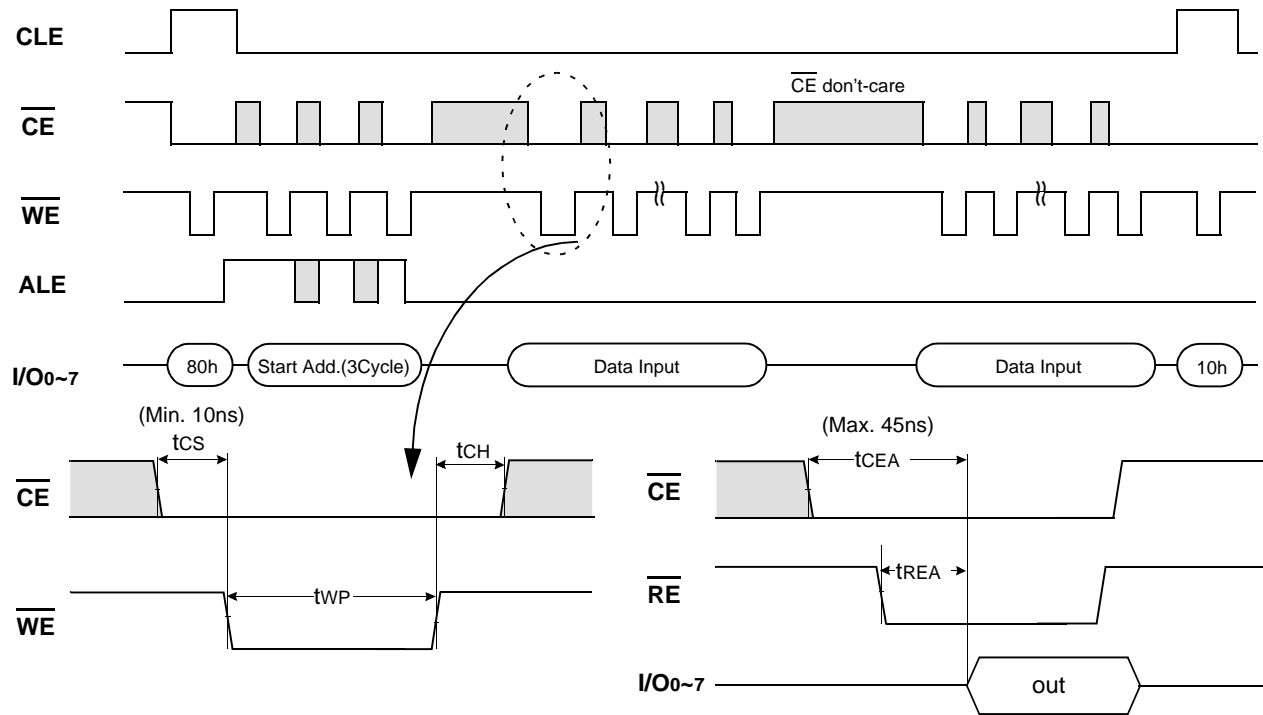
Timing requirements : If $\overline{CE}$ is exerted high during sequential data-reading, the falling edge of $\overline{CE}$ to valid data(tCEA) must be kept greater than 45ns.

Figure 4. Read Operation with $\overline{CE}$ don't-care.

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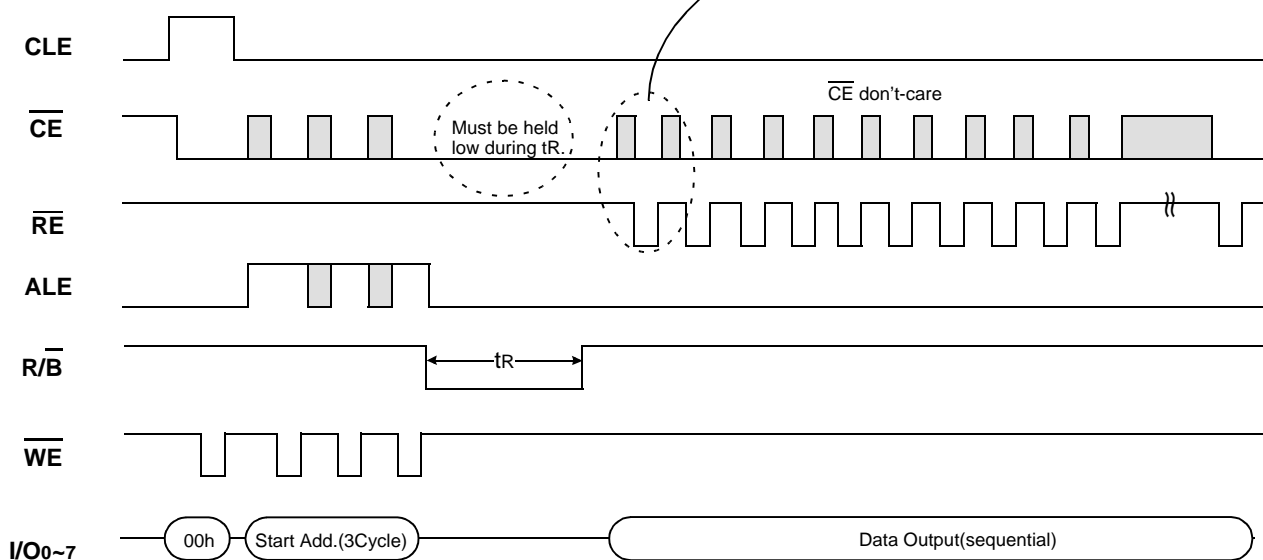
* Command Latch Cycle
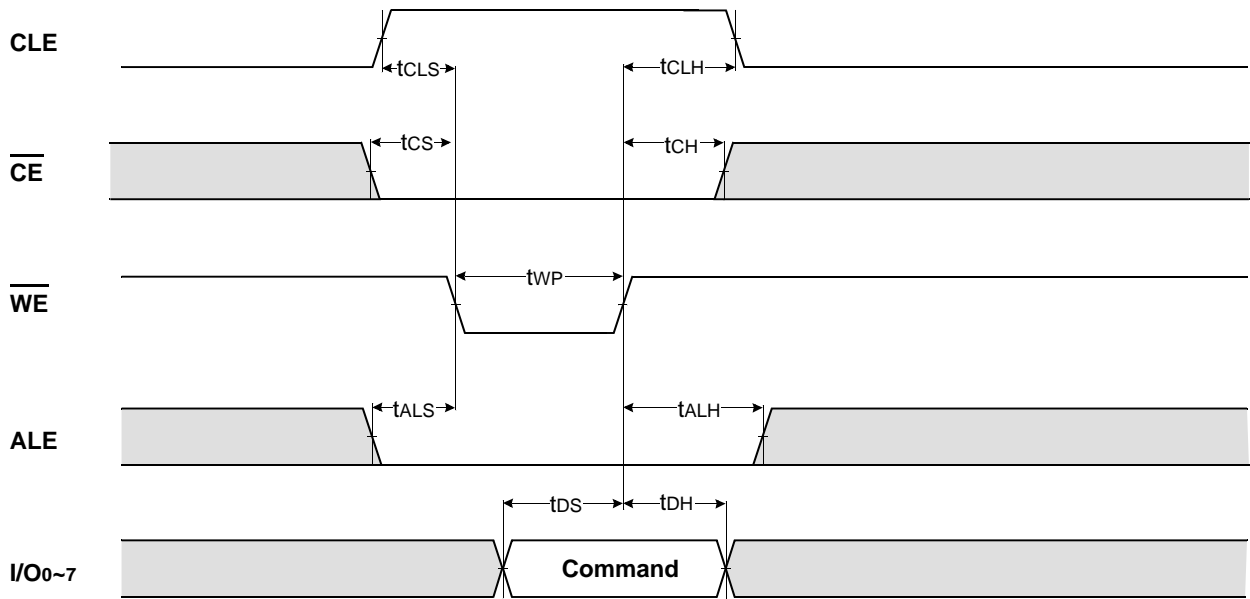
* Address Latch Cycle
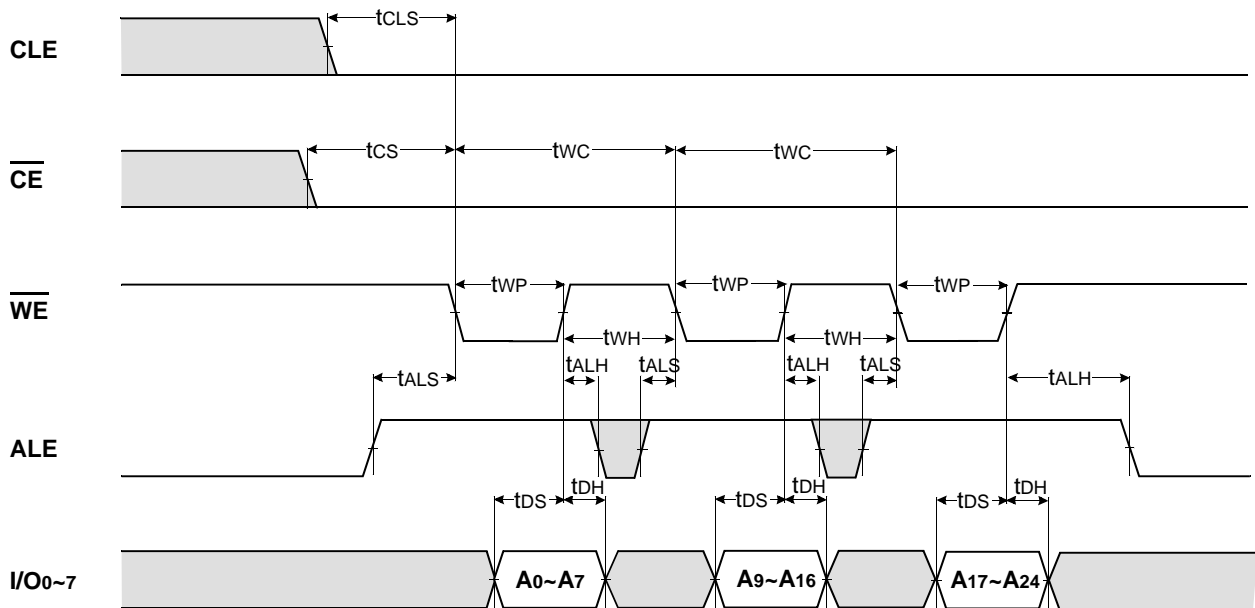
* Input Data Latch Cycle
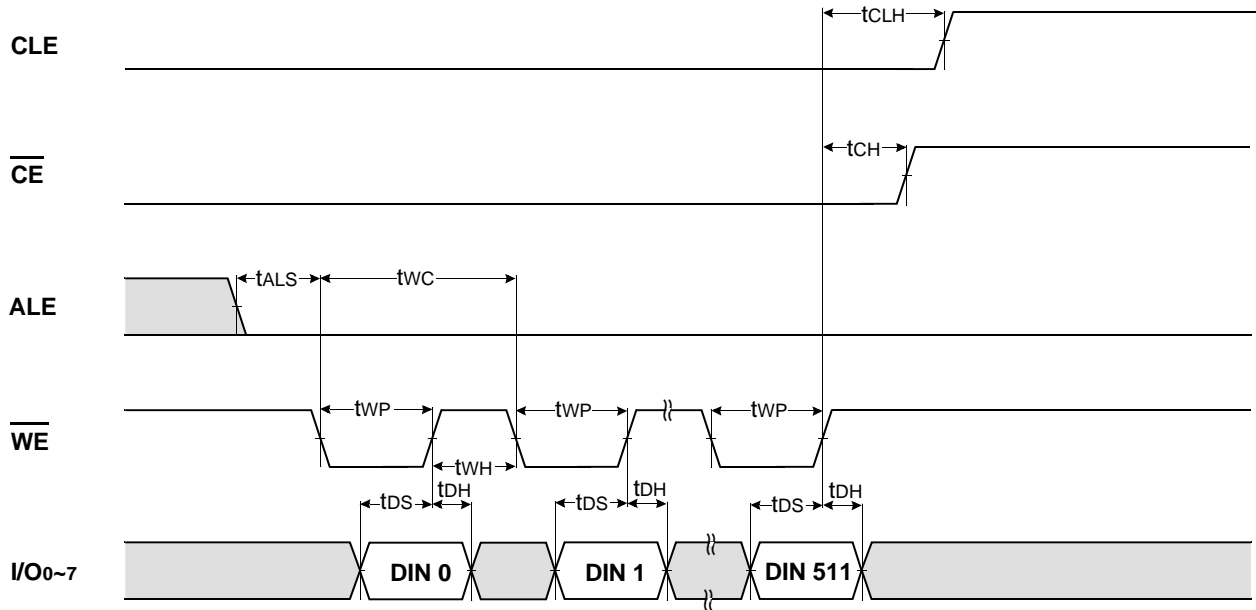
* Serial access Cycle after Read(CLE=L, $\overline{\text{WE}}$=H, ALE=L)
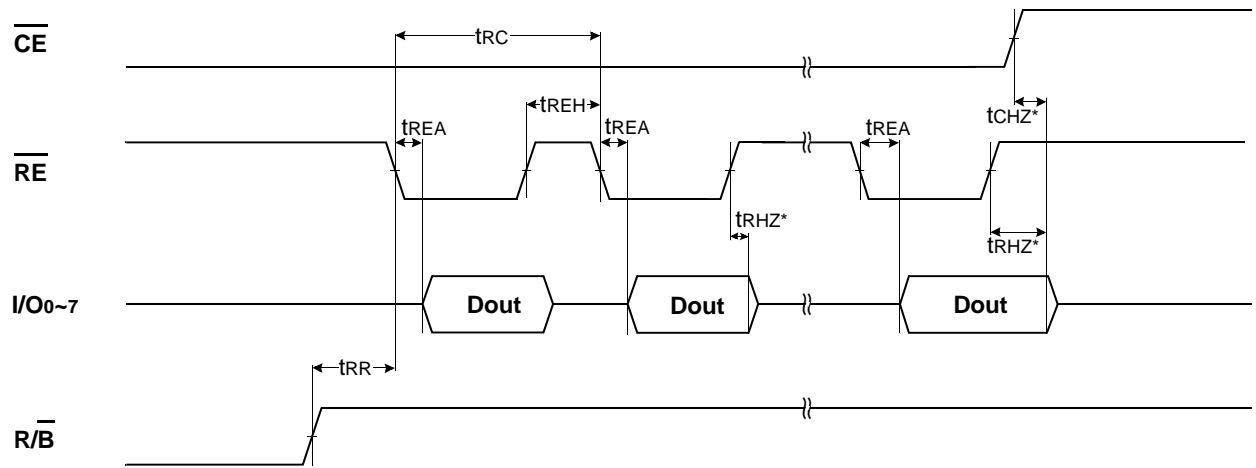
NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

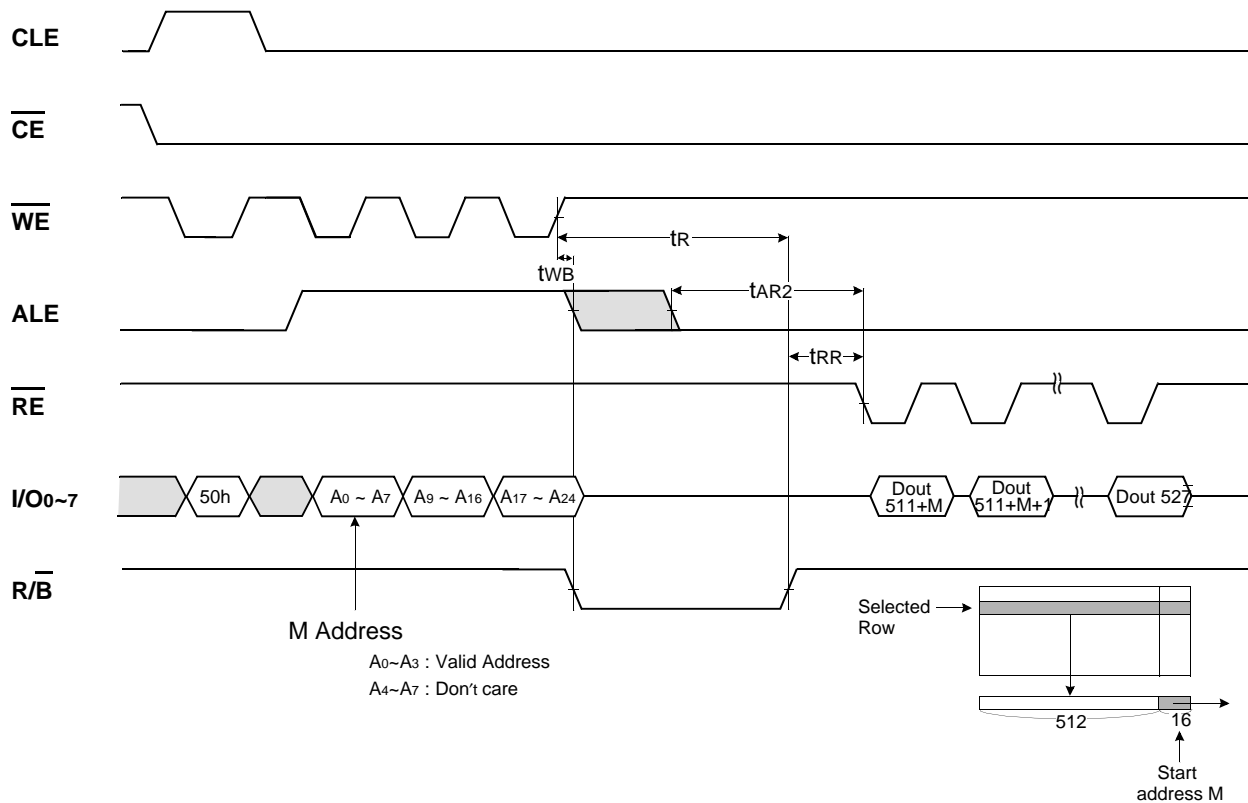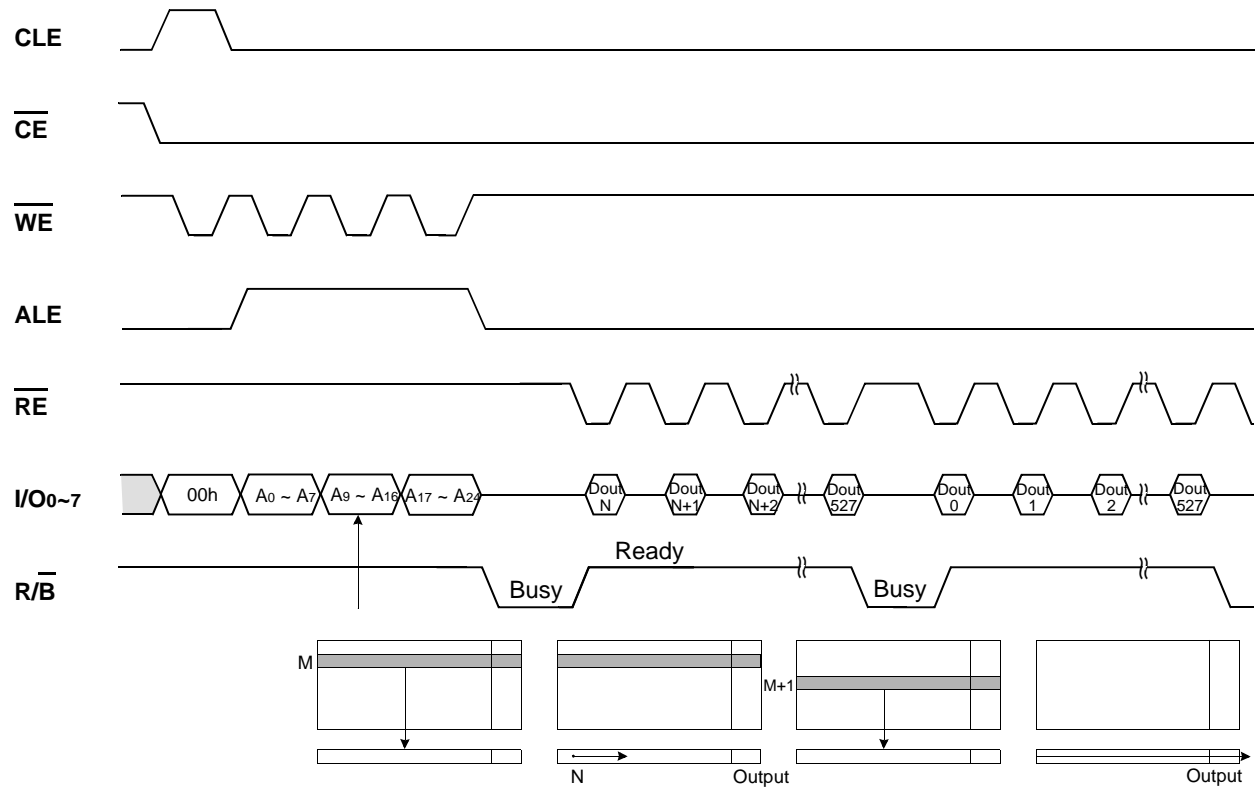*** Status Read Cycle**
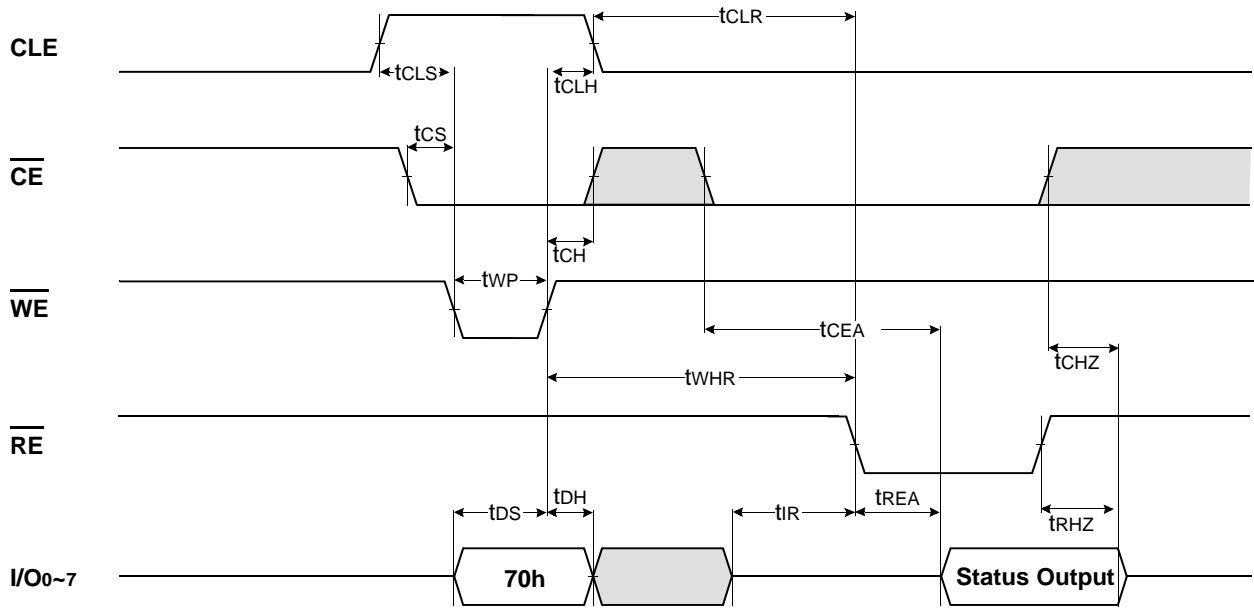
READ1 OPERATION(READ ONE PAGE)

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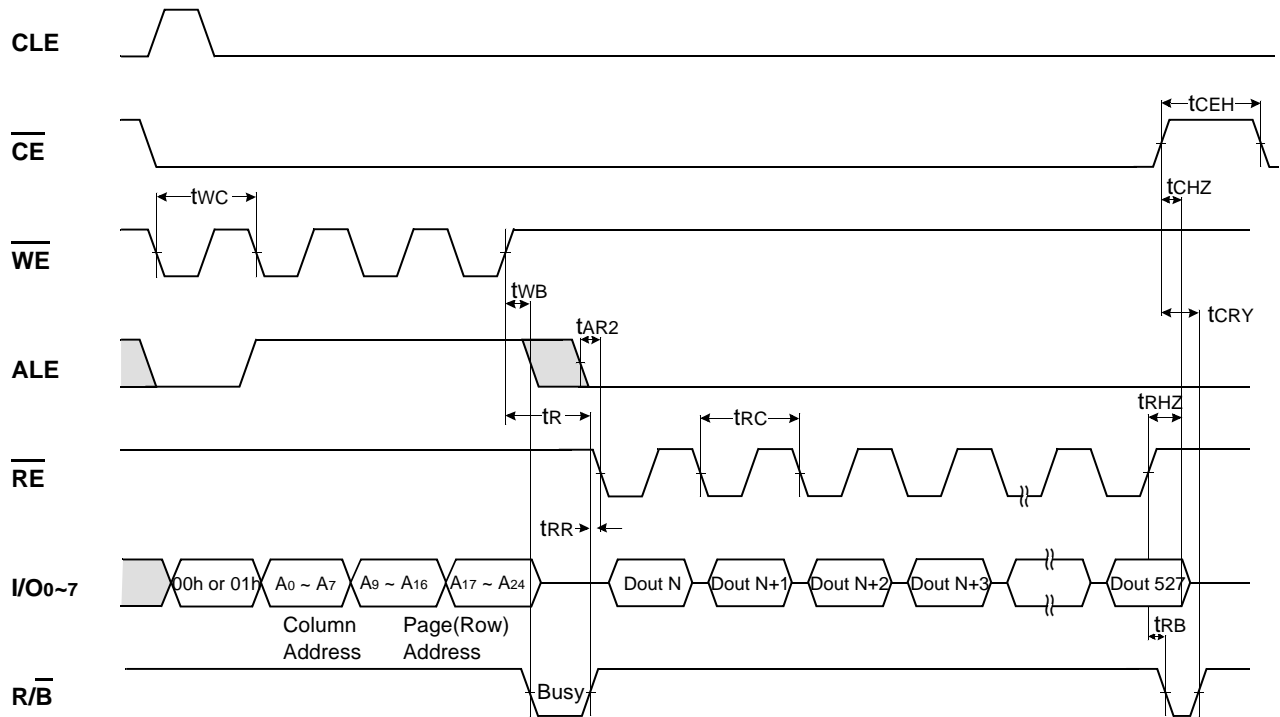
READ1 OPERATION (INTERCEPTED BY $\overline{CE}$)

CLE

$\overline{CE}$

$\overline{WE}$

t_{WB}

ALE

t_{AR2}

t_{CHZ}

t_R

$\overline{RE}$

t_{RC}

t_{RR}

I/O0~7

| 00h or 01h | A0 ~ A7 | A9 ~ A16 | A17 ~ A24 | | Dout N | Dout N+1 | Dout N+2 | Dout N+3 |

Column Address   Page(Row) Address

$R/\overline{B}$

Busy

READ2 OPERATION (READ ONE PAGE)

CLE

$\overline{CE}$

$\overline{WE}$

t_R

t_{WB}

ALE

t_{AR2}

t_{RR}

$\overline{RE}$

I/O0~7

| 50h | | A0 ~ A7 | A9 ~ A16 | A17 ~ A24 | | Dout 511+M | Dout 511+M+1 | Dout 527 |

$R/\overline{B}$

M Address

A0~A3 : Valid Address
A4~A7 : Don′t care

Selected Row

512   16

Start address M

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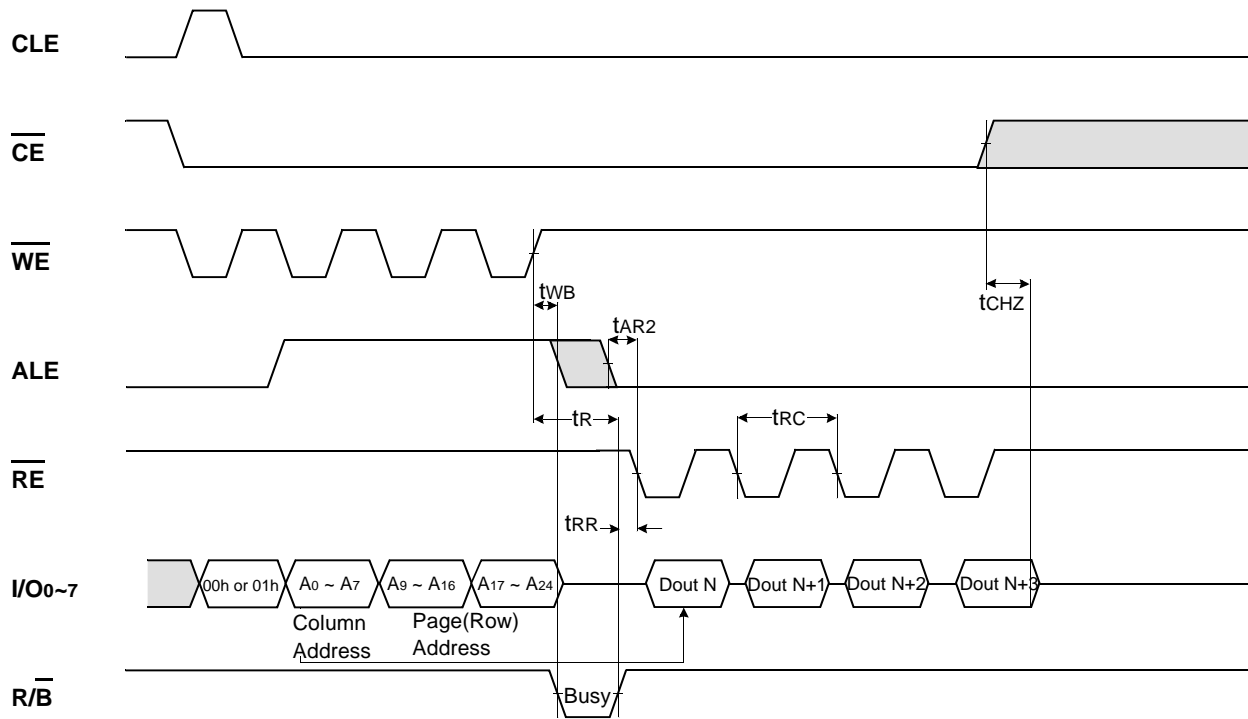
SEQUENTIAL ROW READ OPERATION (WITHIN A BLOCK)

PAGE PROGRAM OPERATION

I/O0=0 Successful Program
I/O0=1 Error in Program

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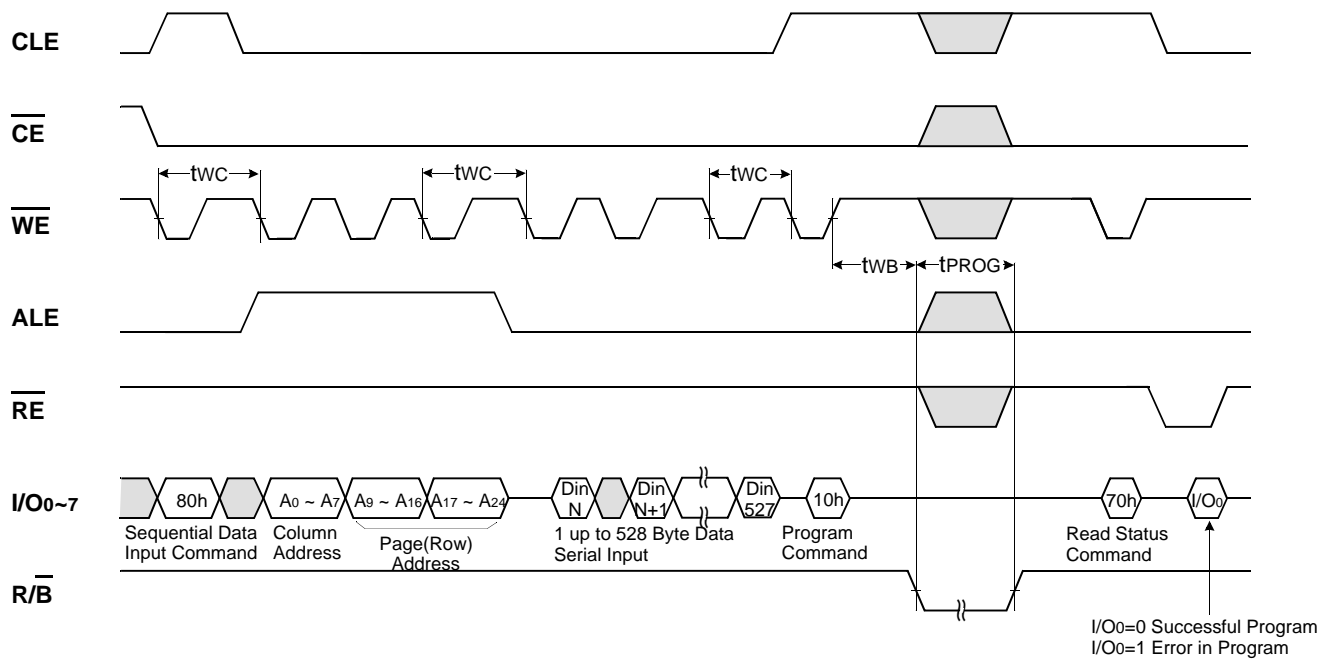
COPY-BACK PROGRAM OPERATION
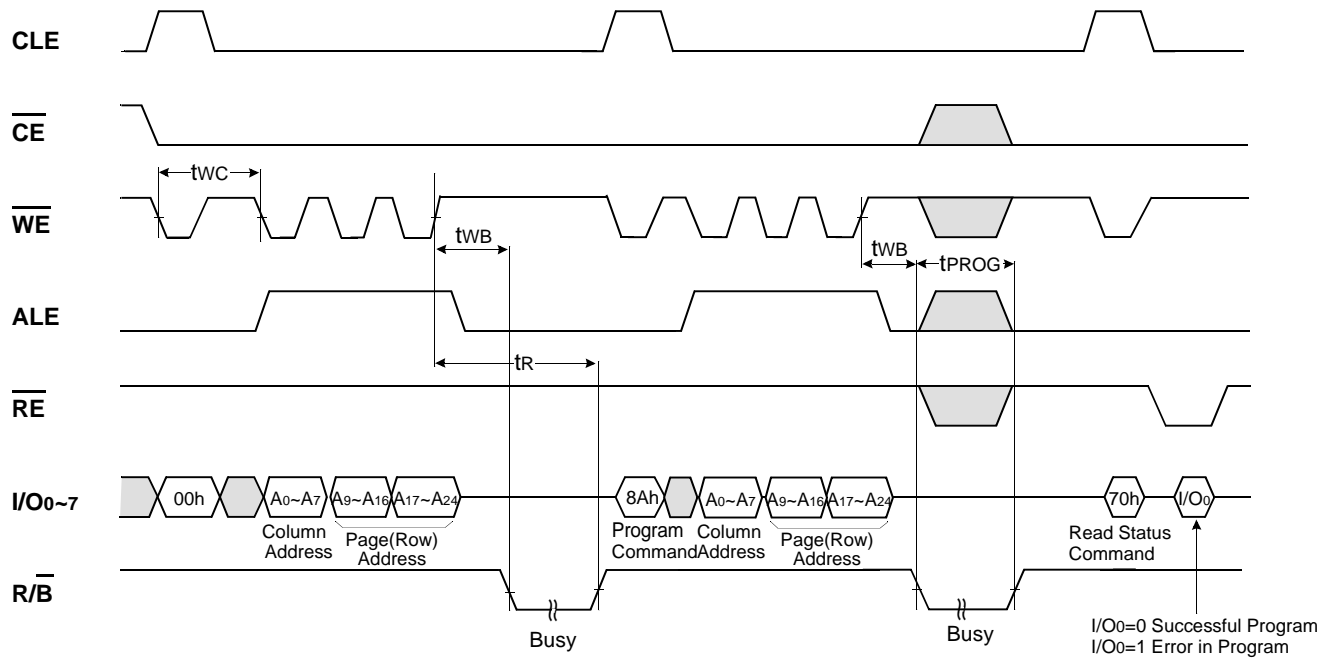
BLOCK ERASE OPERATION (ERASE ONE BLOCK)

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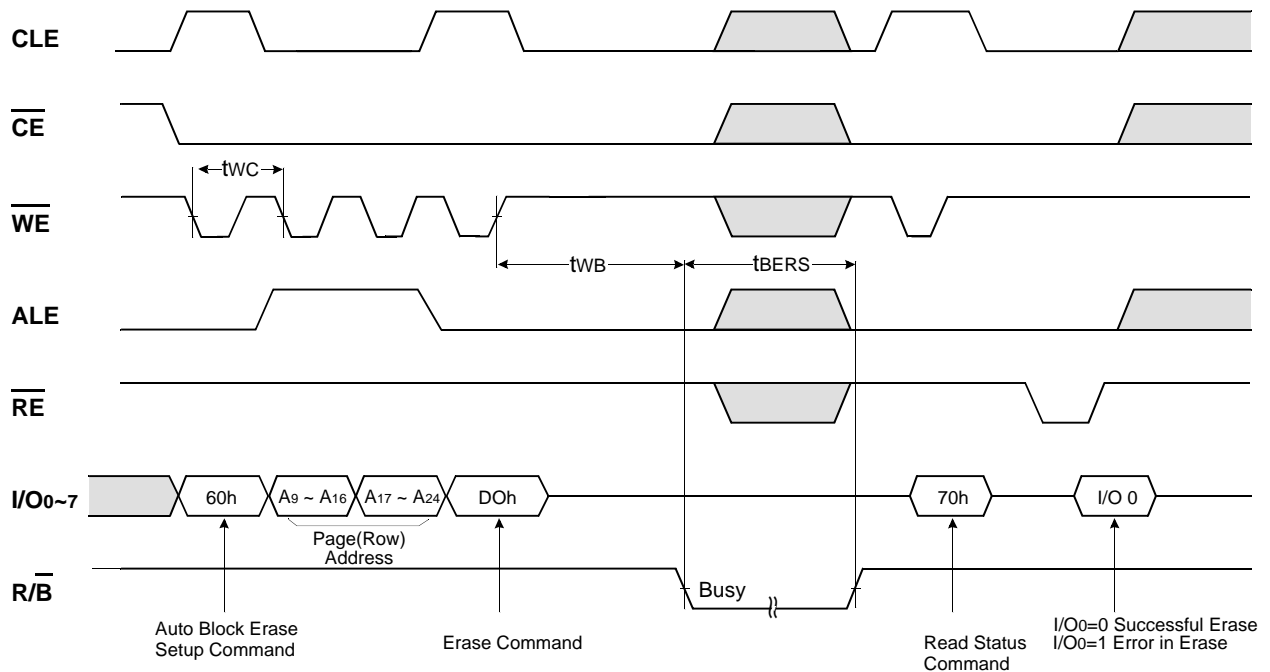
MANUFACTURE & DEVICE ID READ OPERATION

```
CLE       ___/‾‾\___|←————————— tCLR —————————→|_____

CE     ‾‾‾_____

WE     ‾‾‾‾\__/‾‾‾‾_____/‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾

ALE    _____/‾‾‾‾‾‾‾‾‾‾‾‾‾‾_____

                          |←——— tAR1 ———→|
RE     ‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾\__/‾‾\__/‾‾‾‾‾‾‾‾‾‾

                              tREADID →|←
I/O 0 ~ 7  ──< 90h >────< 00h >──────────< ECh >──< 75h >──

         Read ID Command   Address. 1cycle      Maker Code   Device Code
```

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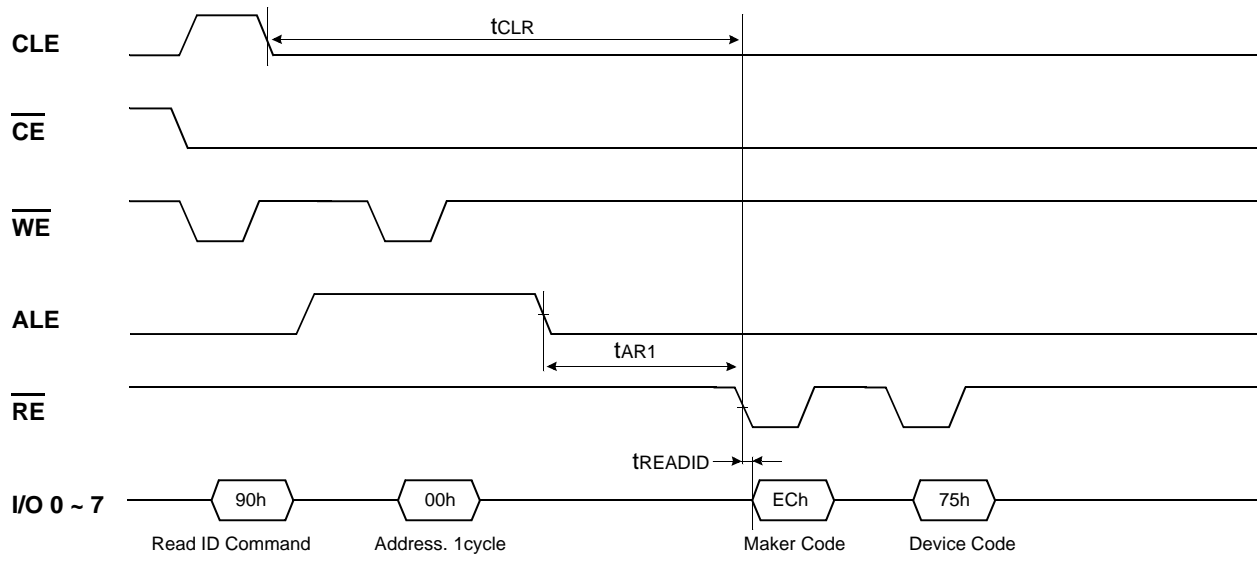
DEVICE OPERATION

PAGE READ

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available : random read, serial page read and sequential row read.

The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 10μs(t_R). The system controller can detect the completion of this data transfer(t_R) by analyzing the output of R/B pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing RE. High to low transitions of the RE clock output the data stating from the selected column address up to the last column address(column 511 or 527 depending on the state of GND input pin).

After the data of last column address is clocked out, the next page is automatically selected for sequential row read. Waiting 10μs again allows reading the selected page. The sequential row read operation is terminated by bringing CE high. The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read2 command with GND input pin low. Addresses A_0 to A_3 set the starting address of the spare area while addresses A_4 to A_7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command(00h/01h) is needed to move the pointer back to the main area. Figures 3 through 6 show typical sequence and timings for each read operation.

Figure 3. Read1 Operation
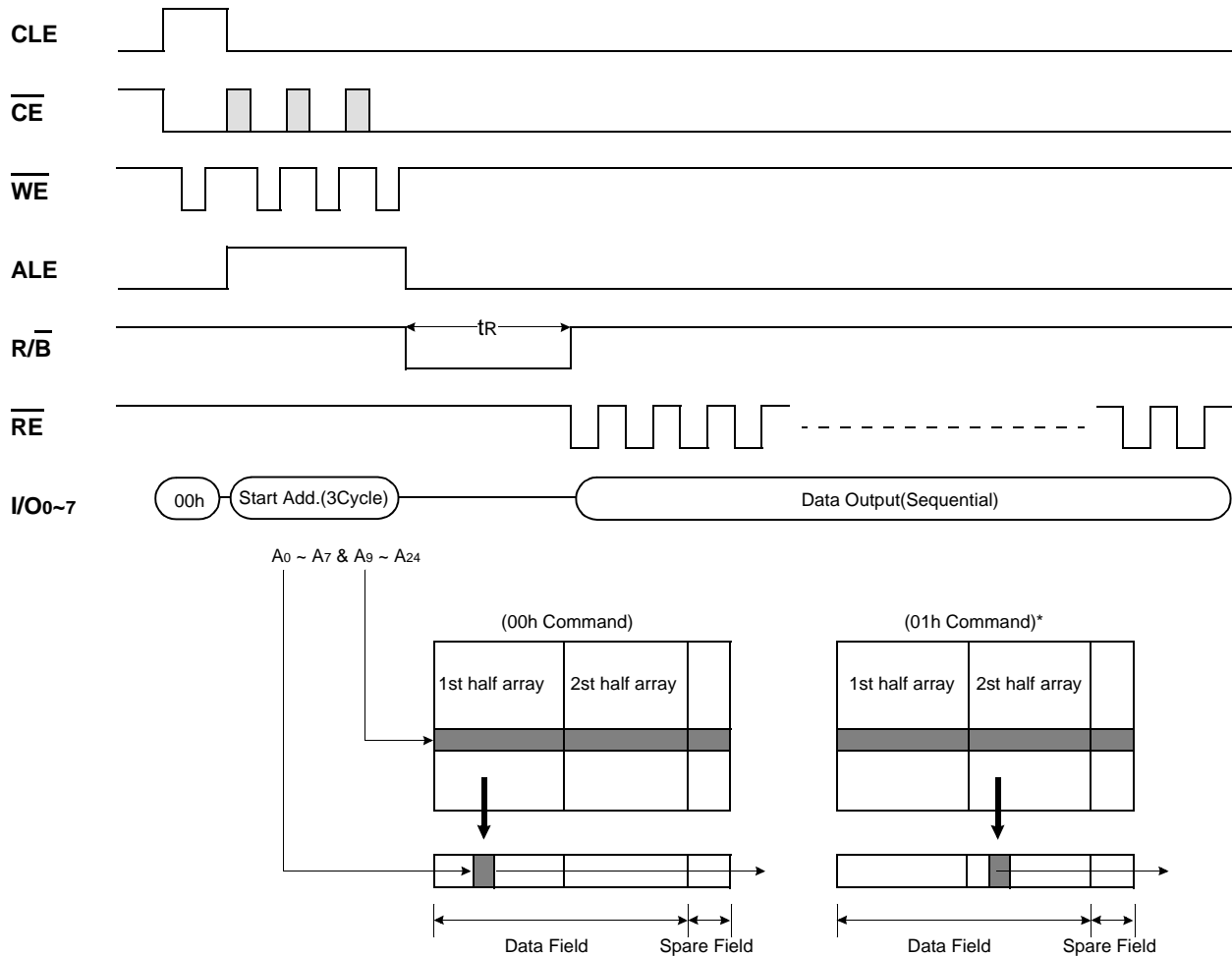
* After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array (00h) at next cycle.
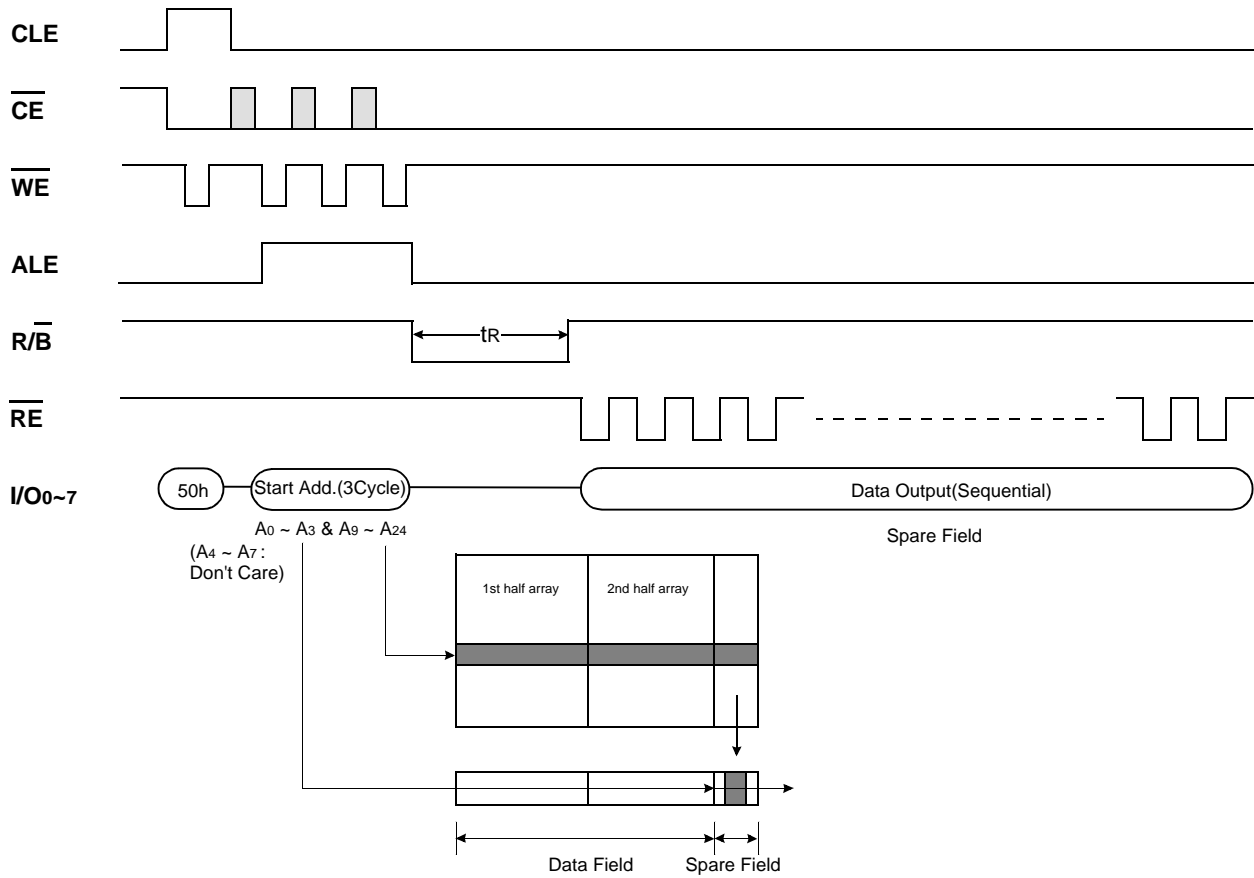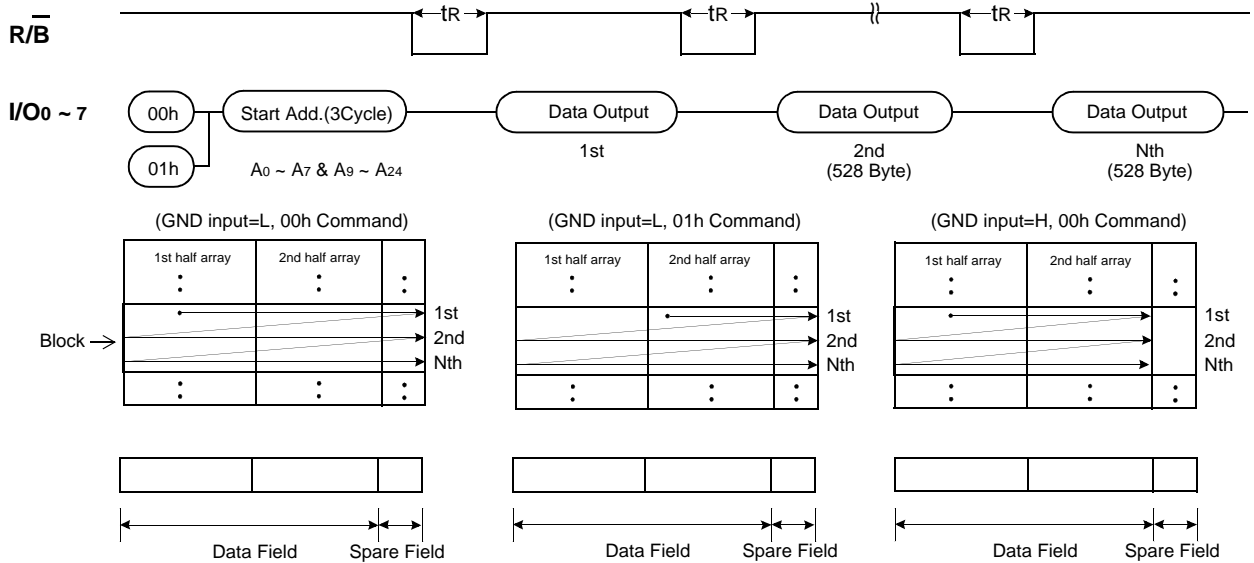
Figure 4. Read2 Operation

Figure 5. Sequential Row Read1 Operation

The Sequential Read 1 and 2 operation is allowed only within a block and after the last page of a block is read-out, the sequential read operation must be terminated by bringing CE high. When the page address moves onto the next block, read command and address must be given.

**Figure 6. Sequential Row Read2 Operation (GND Input=Fixed Low)**
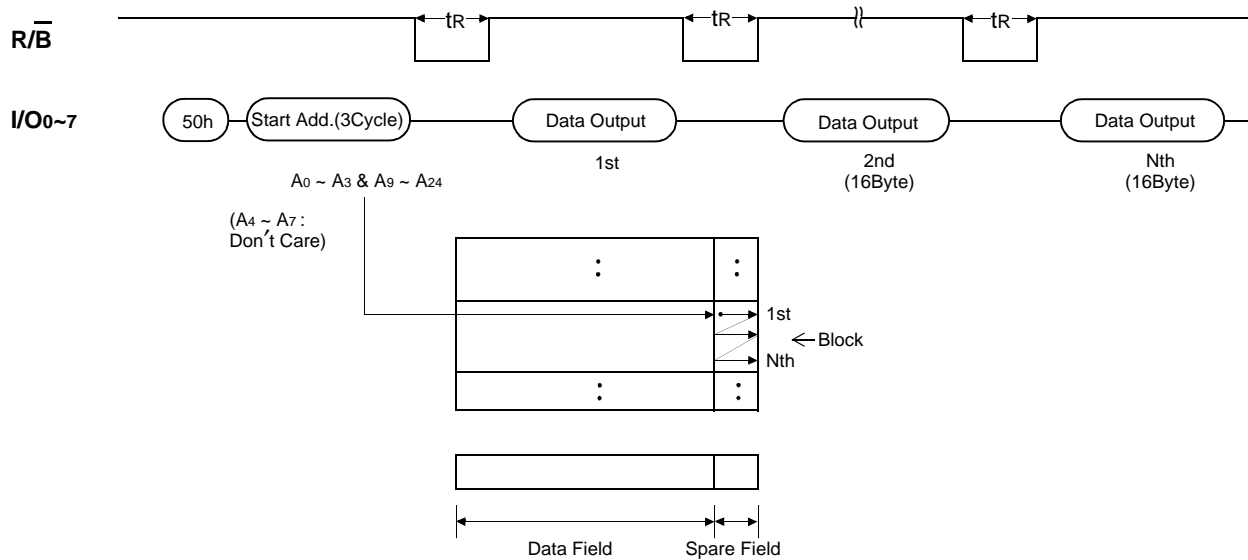
PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programing of a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation should not exceed 2 for main array and 3 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropri-ate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes.
The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the three cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded.The Page Program confirm com-mand(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the pro-gramming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 7). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 7. Program Operation
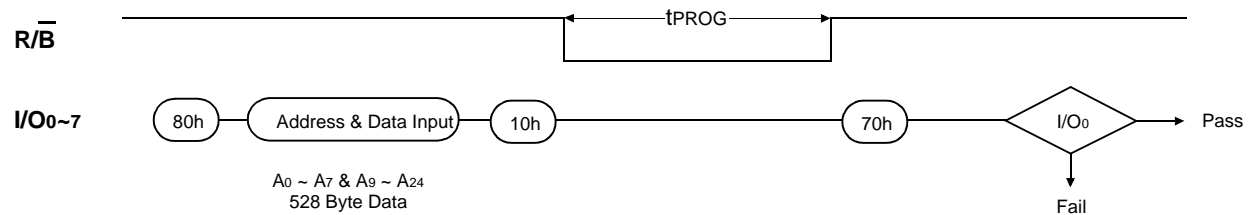
COPY-BACK PROGRAM

The copy-back program is configured to quickly and efficiently rewrite data stored in one page within the array to another page within the same array without utilizing an external memory. Since the time-consuming sequently-reading and its re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command with the address of the source page moves the whole 528byte data into the internal buffer. As soon as the Flash returns to Ready state, copy-back programming command "8Ah" may be given with three address cycles of target page followed. The data stored in the internal buffer is then programmed directly into the memory cells of the destination page. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. Since the memory array is internally partitioned into two different planes, copy-back program is allowed only within the same memory plane. Thus, A14, the plane address, of source and destination page address must be the same. **"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, two bit error correction is recommended for the use of Copy-Back operation."**

Figure 8. Copy-Back Program Operation
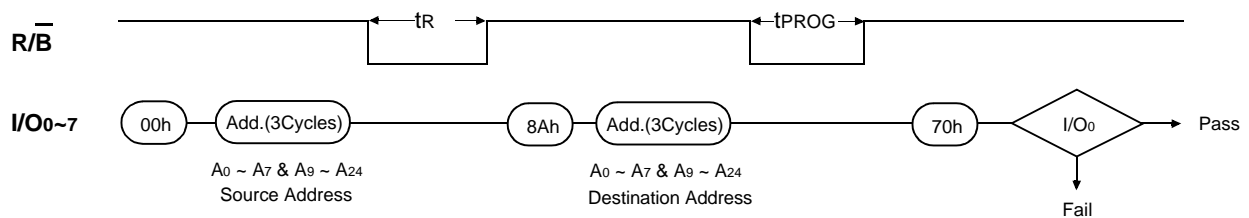
BLOCK ERASE

The Erase operation is done on a block(16K Byte) basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address A14 to A24 is valid while A9 to A13 is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 8 details the sequence.

Figure 9. Block Erase Operation
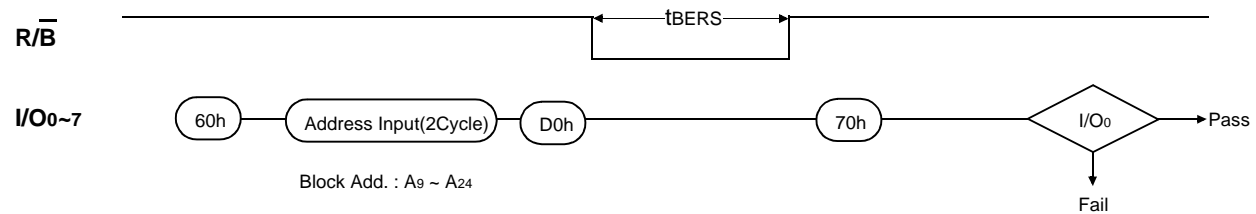
READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

Table2. Read Status Register Definition

I/O #	Status	Definition
I/O 0	Program / Erase	"0" : Successful Program / Erase
		"1" : Error in Program / Erase
I/O 1		"0"
I/O 2		"0"
I/O 3	Reserved for Future Use	"0"
I/O 4		"0"
I/O 5		"0"
I/O 6	Device Operation	"0" : Busy "1" : Ready
I/O 7	Write Protect	"0" : Protected "1" : Not Protected

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECh), and the device code (75h) respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 10 shows the operation sequence.

Figure 10. Read ID Operation
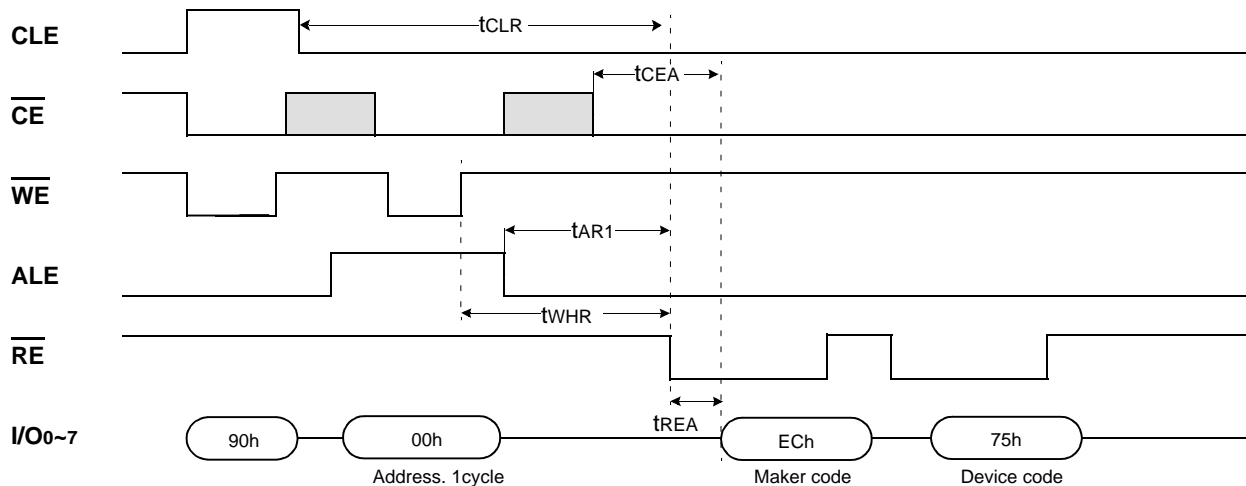
RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to table 3 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Refer to Figure 11 below.

Figure 11. RESET Operation

Table3. Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

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READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 12). Its value can be determined by the following guidance.
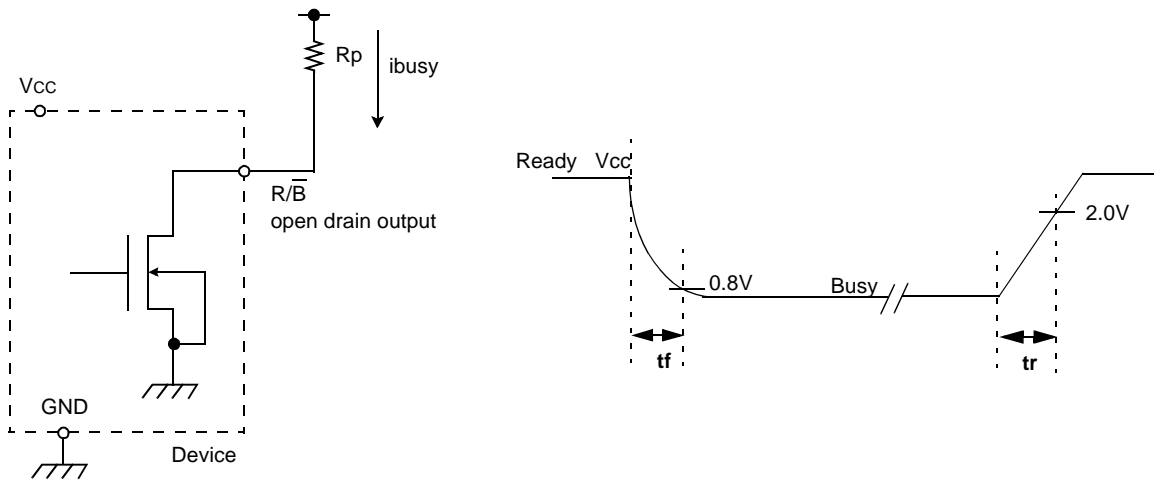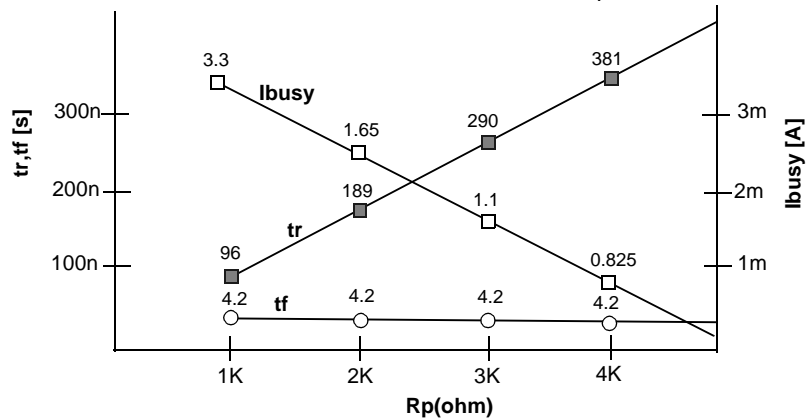

Fig 12   Rp vs tr ,tf &   Rp vs ibusy

@ Vcc = 3.3V, Ta = 25°C , C_L = 100pF

Rp value guidance

$$Rp(min) = \frac{Vcc(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Data Protection & Powerup sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down and recovery time of minimum 1μs is required before internal circuit gets ready for any command sequences as shown in Figure 13. The two step command sequence for program/erase provides additional software protection.

Figure 13. AC Waveforms for Power Transition
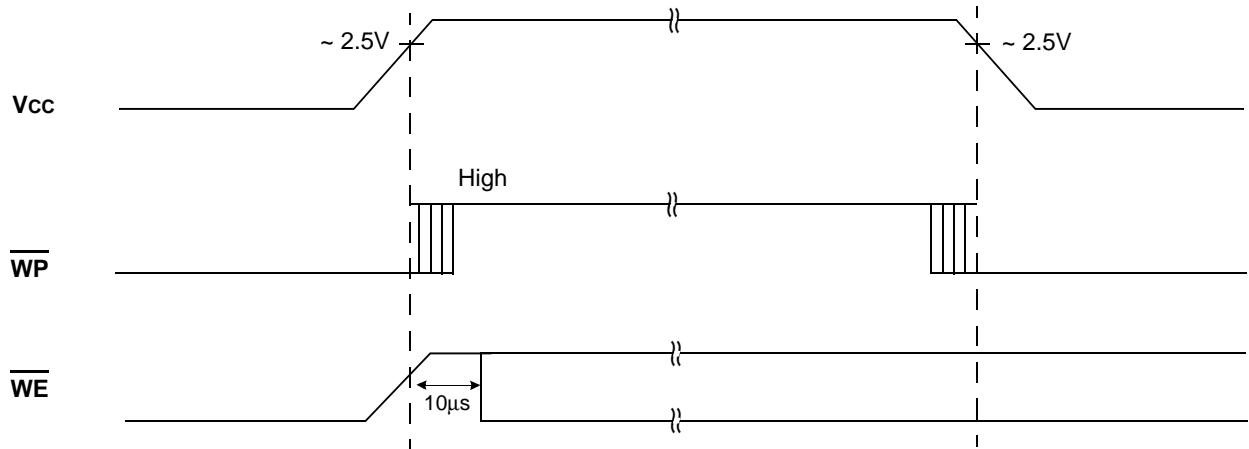
PACKAGE DIMENSIONS

48-PIN LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)