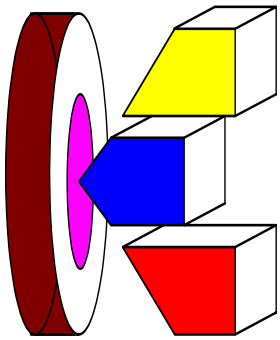


Key Technology Corp.

FC1325N

Single Chip USB Flash Drive Controller

General Descriptions:

The KTC-FC1325N single chip controller is designed for the high capacity and high performance USB Interface Flash Drives. The controller is fully compatible with USB 1.1/2.0 interface, and support the USB Mass Storage Command Protocol.

The controller (LQFP–64) support up to 8 Toshiba/Samsung NAND type Flash Memory devices without any additional circuit. On the other hand, the controller (LQFP-48) can support up to 4 Toshiba/Samsung NAND type Flash Memory devices without any additional circuits. The KTC-FC1325N supports all the control signals to execute read/write/erase operation for flash memory chip.

Features:

1. USB Interface:

1) Support Standard USB (Universal Serial Bus) interface.
2) Fully compatible with USB Spec. 1.1/2.0
3) Support USB Mass Storage Command Protocol.
4) High Speed (480 Mbits/sec), Full Speed (12 Mbits/sec) and Low Speed (1.5 Mbits/sec) transfer support.
5) 4 End points support: Control, Interrupt, Bulk-In, and Bulk-Out.
6) Dual 64 Bytes FIFO for Bulk In, Bulk Out Data Transfer.
7) USB Power saving support.

2. Error Correction Logic:

1) Data Interleave to 2 for each 256 Bytes.
2) Error Correction of 1 Byte random error per 128 Bytes of data.
3) Automatic on-the-fly, in-buffer error correction.

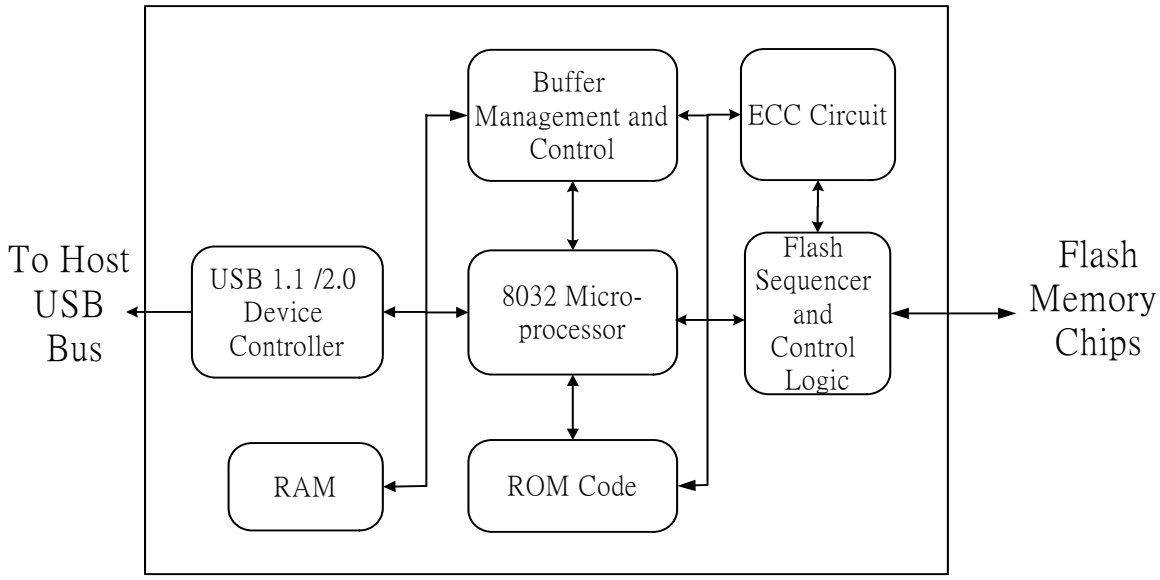
3. Flash Memory Control:

1) Flash Sequencer Logic to support all the control signals to execute read/write/erase operation automatically.
2) Flash Write Protect control support.
3) Support Samsung/Toshiba 32/64/128/256/512/1024/2048/4096 Mbits NAND type flash memories.
4) 8-bit Flash Data I/O.

4. Miscellaneous:

1) +3.3V single power supply.
2) Available in 48-lead LQFP package, 64-lead LQFP package.

Functional Block Diagram:



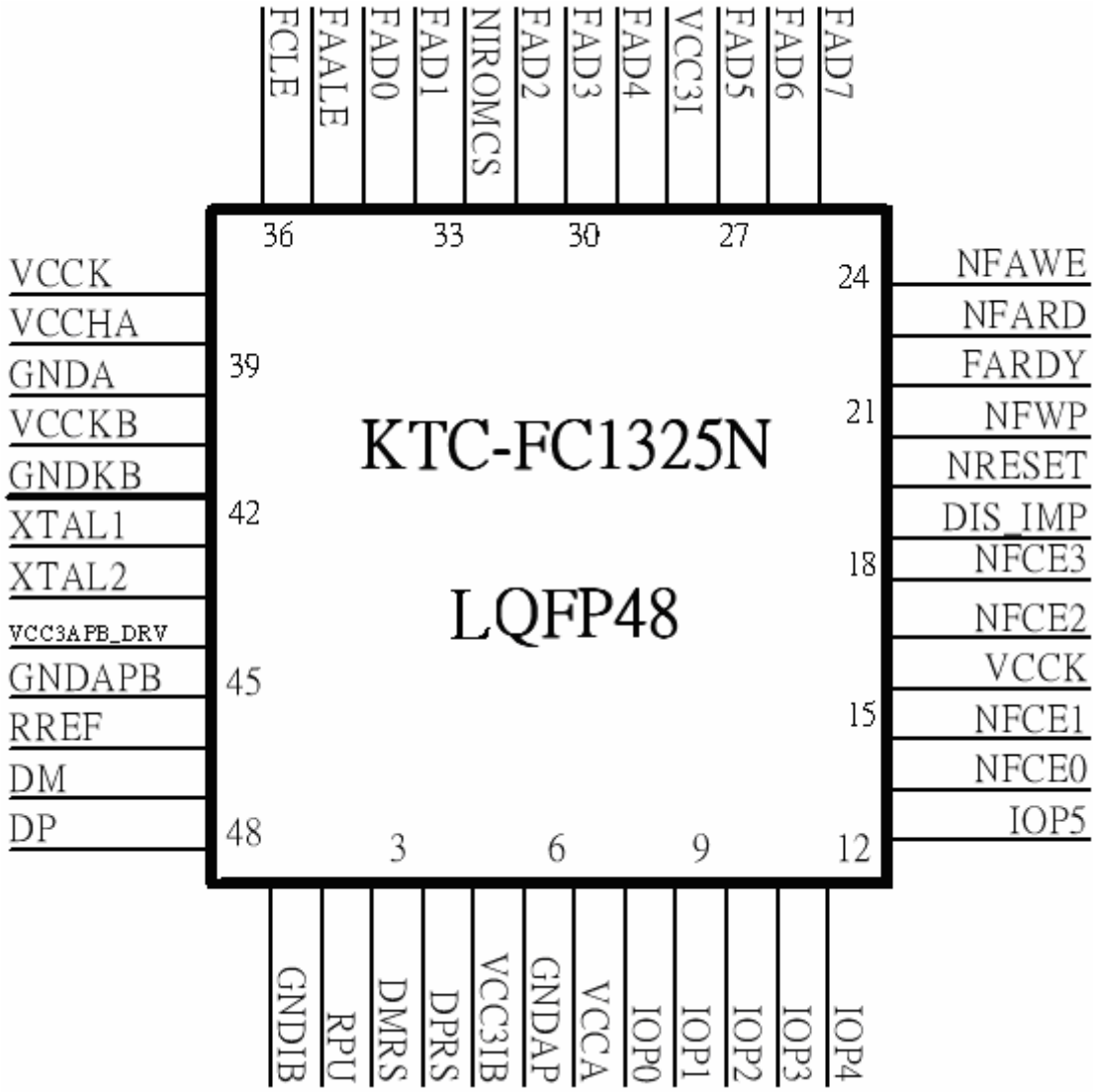
FC1325N Pins Assignment: total 48 pins/ 64 pins (LQFP48/ LQFP 64)

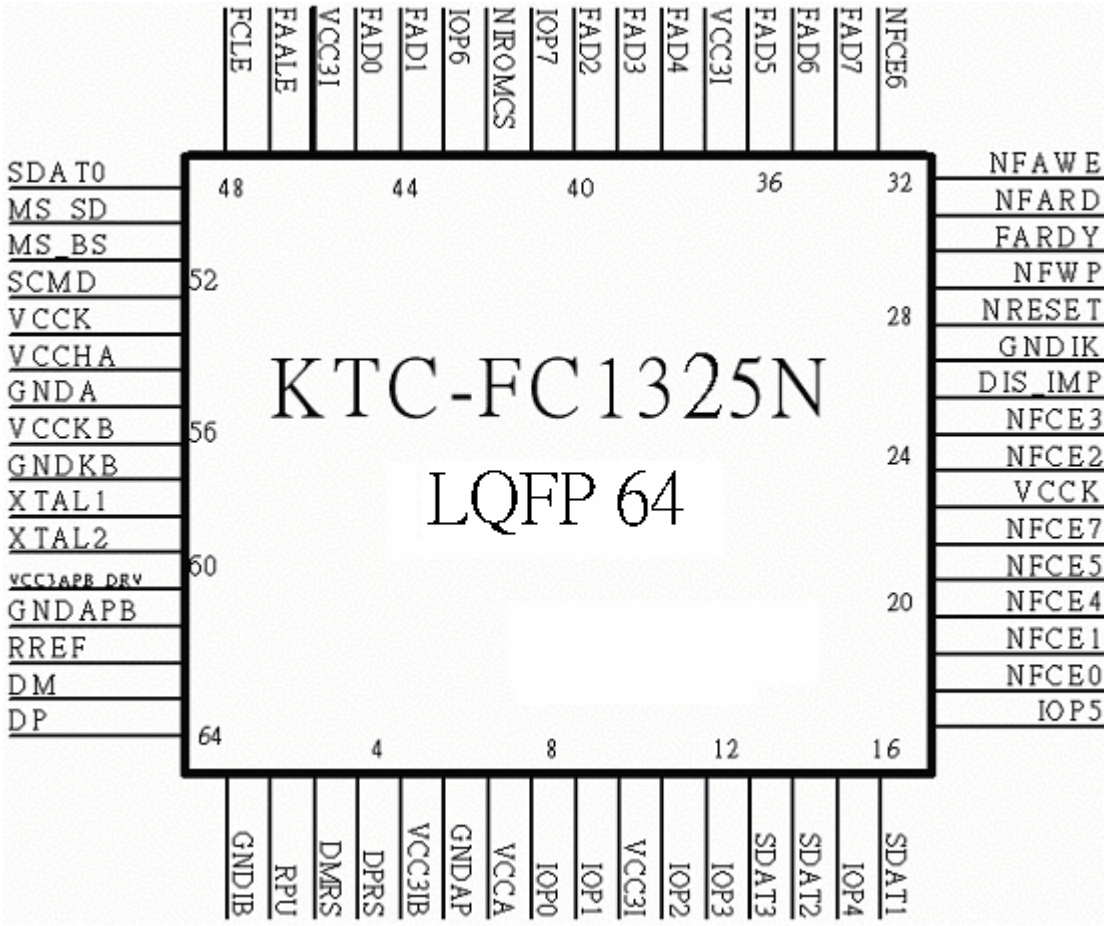
LQFP 48 Pin #	LQFP 64 Pin #	Type 48 Pins 64 Pins	Pin Name 48 Pins 64 Pins	Description 48 Pins 64 Pins
1	1	P	GNDIB	Analog ground supply
2	2	Analog Input	RPU	Connect external resistor (1.5kΩ ± 0.1%) to AVCC (Analog Power 3.3 V)
3	3	I/O	DMRS	USB1.1 data in Data negative pin terminal, connect to external resistor (39Ω ± 0.1%)
4	4	I/O	DPRS	USB1.1 data in Data positive pin terminal, connect to External resistor (39Ω ± 0.1%)
5	5	P	VCC3IB	Digital supply voltage (3.3V)
6	6	P	GNDAP	Analog ground supply
7	7	P	VCCA	Analog supply voltage (3.3V)
8	8	I/O	IOP0	Internal 8032 P1.0
9	9	I/O	IOP1	Internal 8032 P1.1
10	10	I/O P	IOP2 VCC3I	Internal 8032 P1.2 Digital Voltage Supply (3.3V)
11	11	I/O I/O	IOP3 IOP2	Internal 8032 P1.3 Internal 8032 P1.2
12	12	I/O I/O	IOP4 IOP3	Internal 8032 P1.4 Internal 8032 P1.3
13	13	I/O N.C.	IOP5 SDAT3	Internal 8032 P1.5 Reserved
14	14	O N.C.	NFCE0 SDAT2	Flash Device Select 0 Reserved
15	15	O I/O	NFCE1 IOP4	Flash Device Select 1 Internal 8032 P1.4
16	16	P N.C.	VCCK SDAT1	Digital supply voltage (2.5V) Reserved
17	17	O I/O	NFCE2 IOP5	Flash Device Select 2 Internal 8032 P1.5
18	18	O O	NFCE3 NFCE0	Flash Device Select 3 Flash Device Select 0
19	19	I O	DIS_IMP NFCE1	Disable Internal 8032 Flash Device Select 1
20	20	I O	NRESET NFCE4	Chip Reset. (Schmidt) Flash Device Select 4
21	21	O O	NFWP NFCE5	Flash Write Protected Flash Device Select 5
22	22	I O	FARDY NFCE7	Flash Ready/Busy# (Schmidt, PU 50KΩ) Flash Device Select 7
23	23	O P	NFARD VCCK	Flash Read Strobe Digital supply voltage (2.5V)
24	24	O O	NFAWE NFCE2	Flash Write Strobe Flash Device Select 2

25	25	I/O O	FAD7 NFCE3	Flash Data Bus 7 Flash Device Select 3
26	26	I/O I	FAD6 DIS_IMP	Flash Data Bus 6 Disable Internal 8032
27	27	I/O P	FAD5 GNDIK	Flash Data Bus 5 Digital ground supply
28	28	P I	VCC3I NRESET	Digital supply voltage (3.3V) Chip Reset (Schmidt)
29	29	I/O O	FAD4 NFWP	Flash Data Bus 4 Flsh Write Protected
30	30	I/O I	FAD3 FARDY	Flash Data Bus 3 Flash Ready/Busy# (Schmidt, PU 50KΩ)
31	31	I/O O	FAD2 NFARD	Flash Data Bus 2 Flash Read Strobe
32	32	I O	NIROMCS NFAWE	Internal ROM Chip Select Flash Write Strobe
33	33	I/O O	FAD1 NFCE6	Flash Data Bus 1 Flash Device Select 6
34	34	I/O I/O	FAD0 FAD7	Flash Data Bus 0 Flash Data Bus 7
35	35	O I/O	FAALE FAD6	Flash Address Latch Enable Flash Data Bus 6
36	36	O I/O	FCLE FAD5	Flash Command Latch Enable Flash Data Bus 5
37	37	P P	VCCK VCC3I	2.5 V Regulation output Digital Supply Voltage (3.3V)
38	38	P I/O	VCCHA FAD4	High Voltage input of 2.5V Regulator Flash Data Bus 4
39	39	P I/O	GNDA FAD3	Digital ground supply Flash Data Bus 3
40	40	P I/O	VCCKB FAD2	Digital supply voltage (2.5V) Flash Data Bus 2
41	41	P I/O	GNDKB IOP7	Digital ground supply Internal 8032 P1.7
42	42	Analog Input I	XTAL1 NIROMCS	Crystal Oscillator Input (12MHz) Internal ROM Chip Select
43	43	Analog Output I/O	XTAL2 IOP6	Crystal Oscillator Output (12MHz) Internal 8032 P1.6
44	44	P I/O	VCC3APB _DRV FAD1	Analog supply voltage (3.3V) Flash Data Bus 1
45	45	P I/O	GNDAPB FAD0	Analog ground supply Flash Data Bus 0
46	46	Analog Input P	RREF VCC3I	Connect external reference resistor (12.1kΩ ±0.1%) to Analog GND Digital supply voltage (3.3V)
47	47	I/O O	DM FAALE	USB2.0 data pin Data negative pin terminal Flash Address Latch Enable

48	48	I/O O	DP FCLE	USB2.0 data pin Data positive pin terminal Flash Command Latch Enable
	49	N.C.	SDAT0	Reserved
	50	N.C.	MS_SD	Reserved
	51	N.C.	MS_BS	Reserved
	52	N.C.	SCMD	Reserved
	53	P	VCCK	2.5 V Regulation output
	54	P	VCCHA	High Voltage input of 2.5V Regulator
	55	P	GNDA	Digital ground supply
	56	P	VCCKB	Digital supply voltage (2.5V)
	57	P	GNDKB	Digital ground supply
	58	Analog Input	XTAL1	Crystal Oscillator Input (12MHz)
	59	Analog Output	XTAL2	Crystal Oscillator Output (12MHz)
	60	P	VCC3APB_DRV	Analog supply voltage (3.3V)
	61	P	GNDAPB	Analog ground supply
	62	Analog Input	RREF	Connect external reference resistor (12.1kΩ ±0.1%) to Analog GND
	63	I/O	DM	USB2.0 data pin Data negative pin terminal
	64	I/O	DP	USB2.0 data pin Data positive pin terminal

Pin Configurations:




KTC-FC1325N
LQFP 64
FCLE
FAALE
VCC3I
FAD0
FAD1
IOP6
NROMCS
IOP7
FAD2
FAD3
FAD4
VCC3I
FAD5
FAD6
FAD7
NFCE6
SDAT0
MS_SD
MS_BS
SCMD
VCCK
VCCHA
GNDA
VCCKB
GNDKB
XTAL1
XTAL2
VCC3APB_DRV
GNDAPB
RREF
DM
DP
NFAWE
NFARD
FARDY
NFWP
NRESET
GNDIK
DIS_IMP
NFCE3
NFCE2
VCCK
NFCE7
NFCE5
NFCE4
NFCE1
NFCE0
IOP5
GNDIB
RPU
DMRS
DPRS
VCC3IB
GNDAP
VCCA
IOP0
IOP1
VCC3I
IOP2
IOP3
SDAT3
SDAT2
IOP4
SDAT1

Electrical Specifications:

1. DC Characteristics:

1.1 Absolute Maximum Ratings:

Symbol	Parameter	Rating	Units
V_{CC}	2.5V Power supply	-0.3 to 3.0	V
	3.3 Power supply	-0.3 to 3.9	V
V_{IN2}	Input voltage of 2.5V I/O	-0.3 to V_{CC2I}+0.3	V
	Input voltage of 2.5V I/O with 3.3V Tolerance	-0.3 to 3.9	V
V_{IN3}	Input voltage of 3.3V I/O	-0.3 to V_{CC3I}+0.3	V
	Input voltage of 3.3V I/O with 5V Tolerance	-0.3 to 5.5	V
T_{STG}	Storage temperature	-40 to 150	^{o}C

1.2 Recommended Operating Conditions:

Symbol	Parameter	Min.	TYP	Max.	Units
V_{CCk}	Core Power supply	2.25	2.5	2.75	V
V_{CC3I}	Power Supply of 3.3V I/O	3.0	3.3	3.6	V
V_{CC3O}	Power Supply of 3.3V I/O	3.0	3.3	3.6	V

1.3 General DC Characteristics:

Sym.	Parameter	Conditions	Min	Typ	Max	Units
I_{IL}	Input leakage current	no pull up/down	-10		10	μA
I_{OZ}	Tri-state leakage current		-10		10	μA
C_{IN}	Input capacitance			3.1		pF
C_{OUT}	Output capacitance			3.1		pF
C_{BID}	Bi-derectional Buffer capacitance			3.1		pF

1.4 DC Electrical Characteristics:

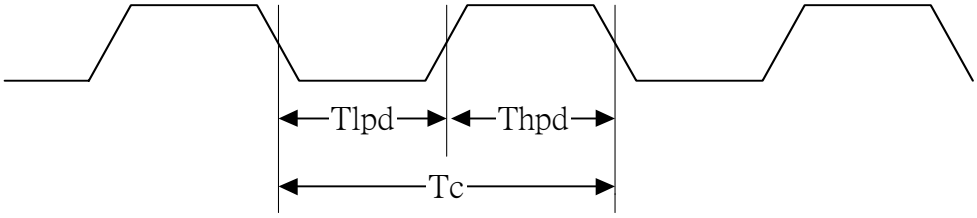
Sym.	Parameter	Min	Typ	Max	Units
V_{CCK}	Core Power Supply	2.25	2.5	2.75	V
V_{CC2I}	Power Supply	3.0	3.3	3.6	V
V_{CC2O}	Power Supply	3.0	3.3	3.6	V
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0			V
Vt-	Schmitt input low voltage	0.8	1.1		V
Vt+	Schmitt input high voltage		1.6	2.0	V
V_{OL}	Output low voltage			0.4	V
V_{OH}	Output high voltage	2.4			V

Rpu/ Rpd	Input pull up/down resistance		75		kΩ

2. AC Characteristics:

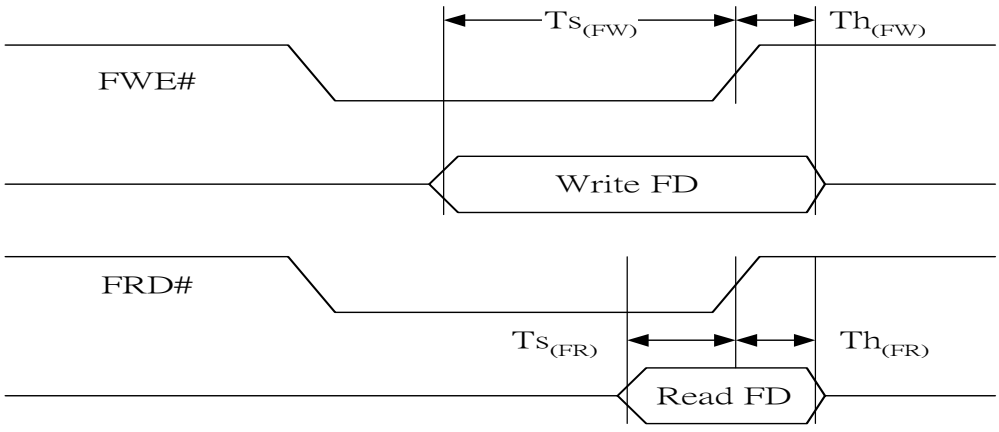
2.1 System clock timing:

Sym.	Description	Min.	Typ.	Max.	Unit
Tc	Clock cycle time		83.3		ns
Tlpd	Clock low pulse duration	0.4Tc		0.6Tc	ns
Thpd	Clock high pulse duration	0.4Tc		0.6Tc	ns



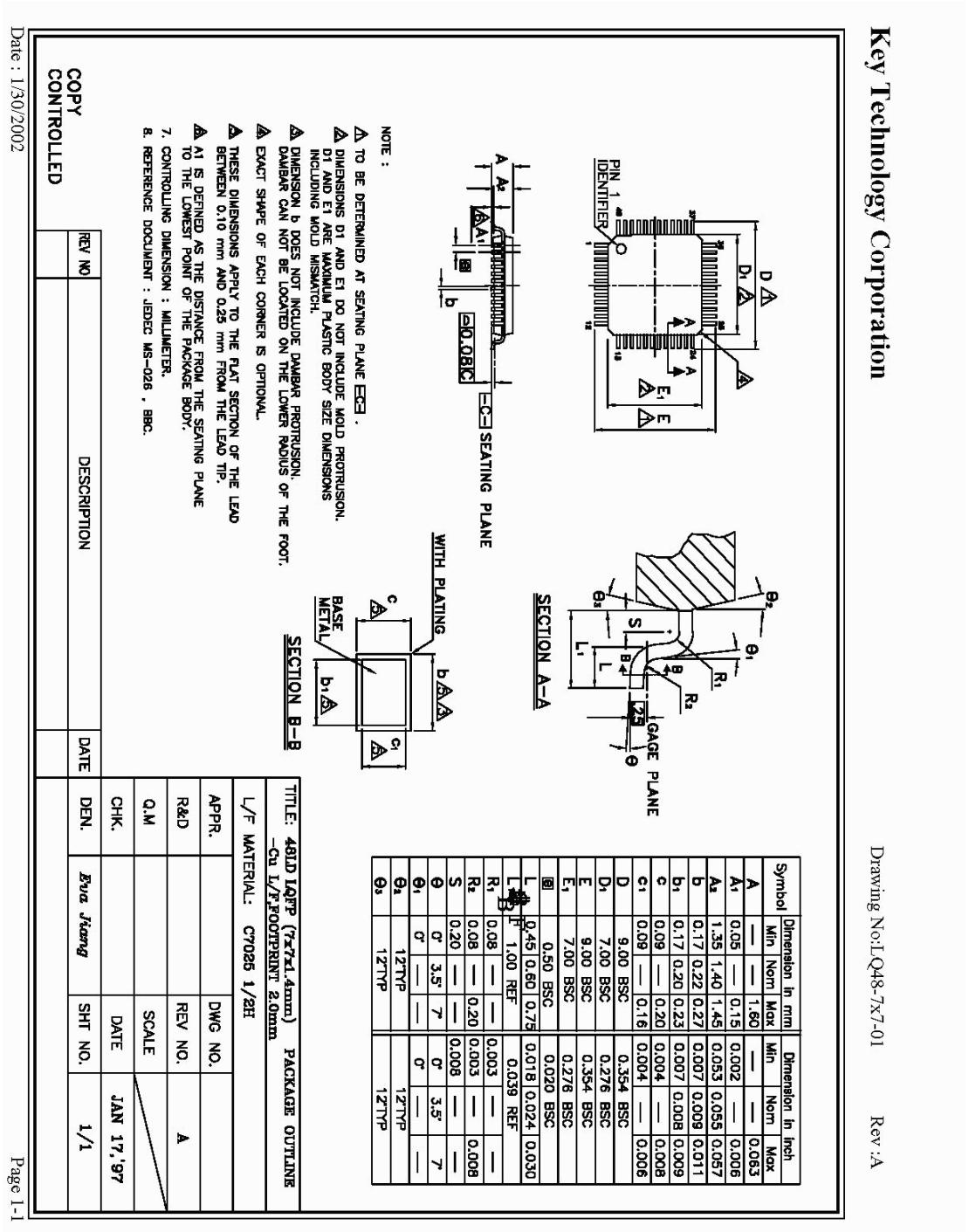
2.2 Flash Read/Write timing:

Sym.	Description	Min.	Typ.	Max.	Unit
$Tc_{(F)}$	Flash Read / Write cycle time		83.3		ns
$Ts_{(FW)}$	FD set up time of FWE#	36.5			ns
$Th_{(FW)}$	FD hold time of FWE#	19			ns
$Ts_{(FR)}$	FD set up time of FRD#	10			ns
$Th_{(FR)}$	FD hold time of FRD#	5			ns

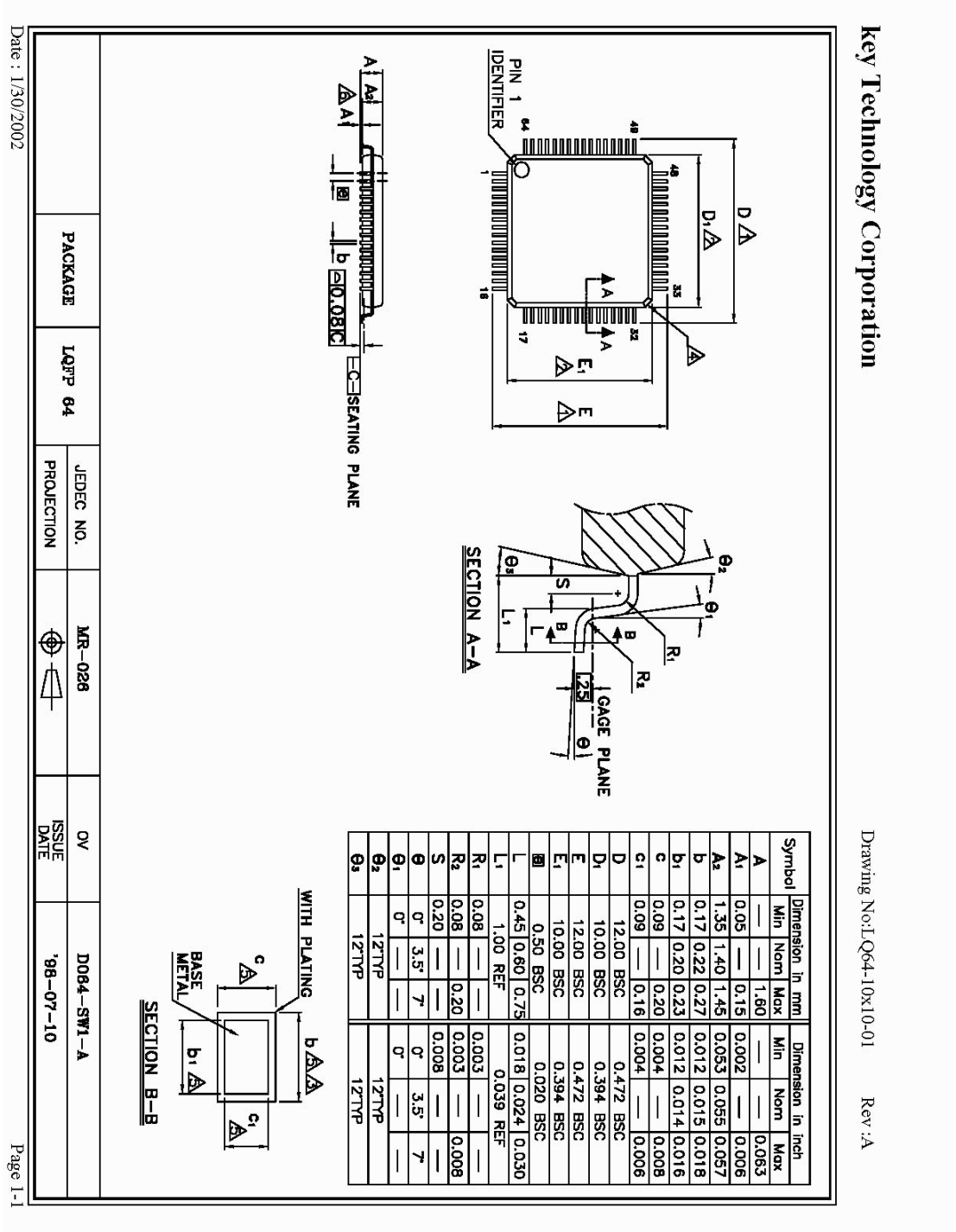


Package Dimensions:

1. LQFP 48



2. LQFP 64



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.012	0.015	0.018
b1	0.17	0.20	0.23	0.012	0.014	0.016
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		